# A low kick-back fully differential dynamic comparator for pipeline analog-to-digital converters

Jose-Angel Diaz-Madrid (1), Gines Domenech-Asensi (2), Johann Hauer (3), Loreto Mateu (3)

[1] Dpto. de Ingenieria y Tecnicas Aplicadas, Centro Universitario de la Defensa en San Javier, Murcia, Spain. mail: jose.diaz@cud.upct.es

[2] Politecnica de Cartagena, Cartagena, Spain

[3] Fraunhofer Institute for Integrated Circuits IIS, Erlangen, Germany

**Abstract:** This study presents a fully differential dynamic comparator with low kick-back noise, an effect caused by voltage variations in the regeneration nodes of these types of circuit. Given their low power dissipation, dynamic comparators are key circuits in analog-to-digital converters (ADCs), especially in pipelined ADCs. The proposed comparator has been simulated and compared with three other comparator topolo-gies. The value of the kick-back noise generated by the proposed circuit is lower than that generated by other conventional dynamic comparators over a wide input range, whilst, simultaneously, showing a low offset voltage error. The dynamic comparator has been implemented in a low-resolution ADC with a resolution of 2.5 efective bits which has been prototyped in a 0.35 $\mu m$ CMOS AMS C35B4 process. Its size is 34 $\mu m$ x 38 $\mu m$.

**Keywords:** CMOS; dynamic comparator; ADC; analog circuit

## 1 | INTRODUCTION

The rapid development of portable electronic devices using wireless data and video protocols has prompted the use of increasingly low power mixed signal circuits, specifically analog-to-digital converters. Given these specifications, pipelined ADCs are popular architectures for high-speed data conversion (10-100 MS/s) at medium to high resolution (8-14 bits) [1]. They are employed in a variety of applications such as imaging or instrumentation systems. Within this architecture, the first few-stages have the greatest impact on the performances of the ADC, the comparator being one of their fundamental building blocks because their speed determines the time margin for settling the signal in the amplifying phase of the ADC. Dynamic comparators are the preferred choice in these ADCs because they can tolerate a high offset error and, also because their power consumption is very low. However, one of the most important disadvantages of these comparators is the noise sources [2,3], particularly the distortion over the input signal because of the kick-back effect, which limits in fact the resolution of the ADC. Kick-back effect or kick-back noise is caused by voltage variations in the regeneration nodes of the dynamic comparator [3] and the coupling of the digital input and output of the circuit to its analog input voltage. Moreover, the regeneration process provides a delay time between the digital input and output of the dynamic comparator. This regeneration time and propagation delay at the digital outputs is solved through digital latches that allow synchronization with the rest of the clock signals generated by the timing circuit. With respect to distortion, this is considered as a non-linearity effect known as kick-back noise. In a pipelined ADC, this noise and in general, the total noise power of a pipeline A/D converter with $k$ stages, referred to its input, is given by:

$$e_{Total}^2 = e_1^2 + \frac{e_2^2}{G_1} + \frac{e_3^2}{G_2} + \cdots + \frac{e_k^2}{\prod_{i=1}^{k-1} G_i} \tag{1}$$

where $e_i^2$ is the noise power at the stage input, and $G_i$ the interstage gain of the $i^{th}$ stage. Because the noise contribution of the subsequent stages is attenuated by the interstage gains of the proceeding stages, the kick-back noise is especially critical in the first stages of the pipelined ADC. Once the topology of the comparator has been tested for the first stage, this is integrated for the rest of the stages of the pipeline ADC. On the other hand, contrary to the noise power, the offset voltage $V_{OS,Comp}$ than can be allowed in the comparators depends exclusively on the topology of the stage and the reference voltage. This error is given by:

$$V_{OS,Comp} = \pm \frac{r}{2^{B_i+r}} V_R \tag{2}$$

where $B_i$ is the digital output of the $i^{th}$ stage and $r$ is the redundancy of the stage. This means that smaller offset voltage would not improve the general performance of the pipelined ADC. Dynamic comparators disclose multiple advantages with respect to other typologies, meaning this does not require any extra preamplifier stage that would imply the addition of static power consumption [3]. Another advantage is that the dynamic comparator does not use additional capacitors, contrary to other publications [4]. Therefore, the use of reference capacitors is not necessary, thereby simplifying the circuit. Besides the aforementioned ones, in the literature there are recent proposals of dynamic comparator designed to reduce the kick back effect. In [5] and [6], three stage comparators are used employing more than 20 transistors each, being the latter circuit able reduce the kick-back noise from 7.6 mV to 5.9 mV. Also in [7], a single ended charge steering dynamic comparator which offers a kick-back noise of 3 mV is described. In [8,9,10] other topologies of dynamic comparators are shown exhibiting different performance, although their kick-back effect reduction is not quantified.

In this short communication, a low kick-back noise dynamic comparator is presented. The value of the kick-back noise generated by the proposed circuit is lower than that generated by other conventional dynamic comparators over a wide input range, whilst, simultaneously, the offset voltage error is remained in the working range and the power consumption is extremely low. The rest of the paper is organised as follows: Section 2 describes the implementation of the dynamic comparator. The proposed architecture is simulated in Section 3. Section 4 presents the experimental results obtained from the implementation of the stages of an 11-bit pipelined ADC. Finally, conclusions are drawn up in Section 5.

## 2 | CIRCUIT IMPLEMENTATION

Dynamic comparators are very efficient circuits from a power consumption perspective because they do not need static currents to work properly [3]. Moreover, some dynamic comparators allow the reduction of the global reference voltages that are needed for the analog amplification of a pipelined ADC, because the trip points are internally fixed through the geometrical relationships. This topology reduces the total number of reference voltages, simplifies circuits such as bandgaps and analog buffers and, also reduces the complexity of the physical layout. Fig. 1.a shows the structure of a conventional dynamic comparator [11].

The operation of this circuit is as follows. When the clock signal (CLK) is high, the transistors M5 and M8 are ON and the transistors M12 and M13 are OFF. This effect forces both differential outputs to VDDA. Consequently, M6 and M7 are OFF and M10 and M11 are ON. In this state, the dynamic comparator is not consuming energy and the transistors M1, M2, M3 and M4 are in the triode region fulfilling the role of these transistors as $V_{DS} < V_{GS} - V_T$, where $V_T$ is the threshold voltage, $V_{GS}$ is the gate-source voltage and $V_{DS}$ is the drain-source voltage.

When the clock signal (CLK) goes down, the transistors M12 and M13 are turned ON and M5 and M8 are turned OFF. This means that at the end of this falling edge, the transistors M5, M6, M7 and M8 are cut off and the transistors M10, M11, M12 and M13 are ON. At this precise point, the outputs voltages will start to turn low or high depending on the polarization of the transistors M1, M2, M3 and M4 if the rest of the circuit is geometrically symmetrical. Therefore, considering that transistors M1, M2, M3 and M4 are in the triode region, if the conductance $G_{M1-M2}$ formed by the transistors M1 and M2 is higher than the parallel conductance $G_{M3-M4}$ formed by M3 and M4, then $V_{OUT}^+$ will turn low faster than $V_{OUT}^-$ and $V_{OUT}^+$ will turn on the transistor M7 forcing the output $V_{OUT}^-$ to high. Otherwise, if $V_{OUT}^-$ turns low faster than $V_{OUT}^+$, then $V_{OUT}^+$ will be forced to high. Given that once the comparison is made and the dynamic comparator reaches a stable state in the voltages output, there will be no static current flowing through the dynamic comparator. The delay between the clock signal and the digital outputs is caused by the regeneration time. This propagation delay is solved through digital latches that allow the synchronizing with the rest of the clock signals generated by the timing circuit of the pipeline ADC.

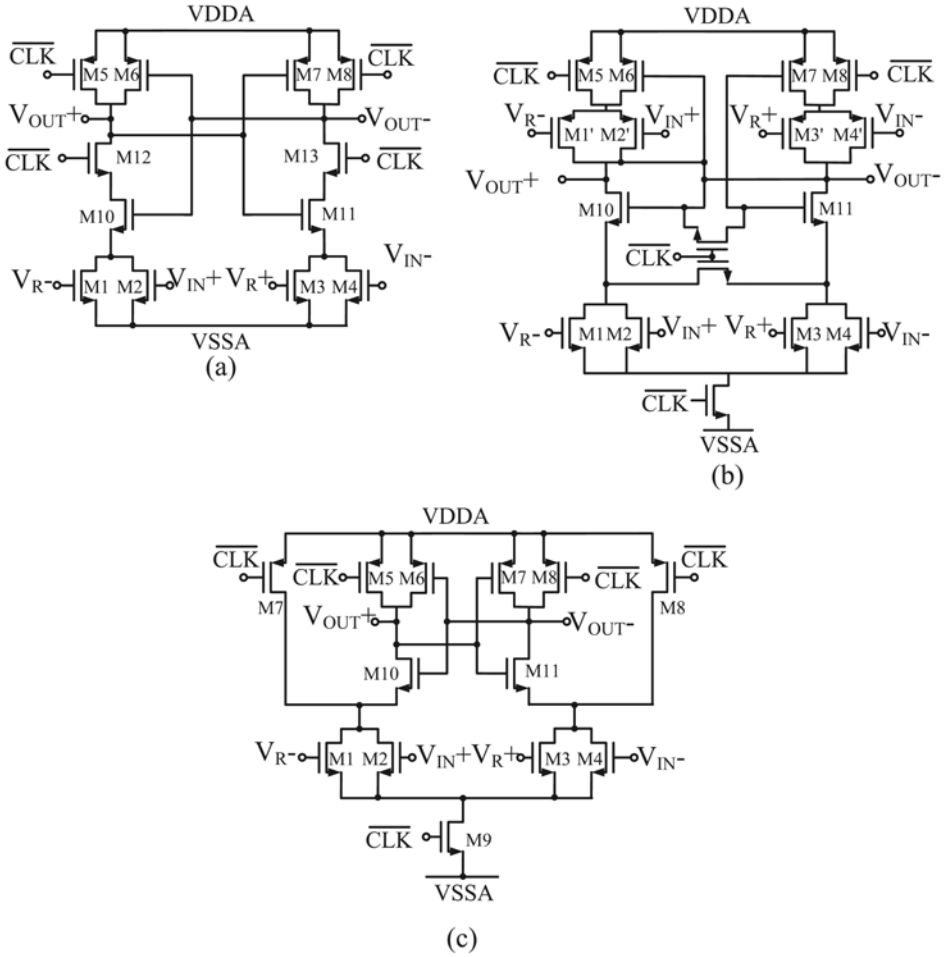


Figure 1 a) Conventional dynamic comparator (CDC), b) Complementary input dynamic comparator (CIDC), c) Low offset dynamic comparator (LODC).

The digital output of the comparator is defined according to the resistance fixed by the input transistors, M1 to M4, connected to the inputs $V_{IN}^{+}$, $V_{IN}^{-}$, and the references $V_R^{+}$ and $V_R^{-}$. Since the structure of the comparator is fully differential, the differential analog inputs are defined as $V_{IN} = V_{IN}^{+} - V_{IN}^{-}-$ and $V_R = V_R^{+} - V_R^{-}$. The input transistors are designed with the following width restrictions: $W_2 = W_4$, $W_1 = W_3$, while all their lengths have the same value. To set up the trip points, the widths of the transistors connected to the analog inputs and the reference voltages are physically configured according to $W_1 = k \cdot W_2$. As a result, the trip point of the dynamic comparator is defined by:

$$V_{IN,TripPoint} = k \cdot V_R \tag{3}$$

The major drawback of this topology is that the offset voltage depends heavily on the process variations. Figs. 1.b-c show alternate topologies of dynamic comparators called, respectively, complementary input dynamic comparator (CIDC)[12] and low offset dynamic comparator (LODC)[13]. They have the advantage of being more robust structures with respect to the offset error. The reason is that CIDC can manage a higher input voltage dynamic range because of the extra *pmos* transistors $M_1' - M_4'$. On the other hand, LODC has a lower input dynamic range ($2\ Vpp$), but this reduces the dependency on the input-referred offset voltage of the matching of M10 and M11 and the input differential pair transistors through the addition of transistors M7, M8 and M9. However, both configurations present a higher kick-back effect than the circuit proposed in this study.

In order to reduce the coupling of the digital input and output of the circuit to the input analog voltage, thereby decreasing the kick-back effect, the circuit proposed in this study (Fig. 2) includes two additional transistors, M12 and M14 to prevent this effect. When CLK goes high, these transistors disconnect the analog input from the cross coupled latch. Moreover, to reduce the offset error, a third transistor, M13, is used to match the voltage at nodes C and D. So, when CLK goes down, the positive feedback

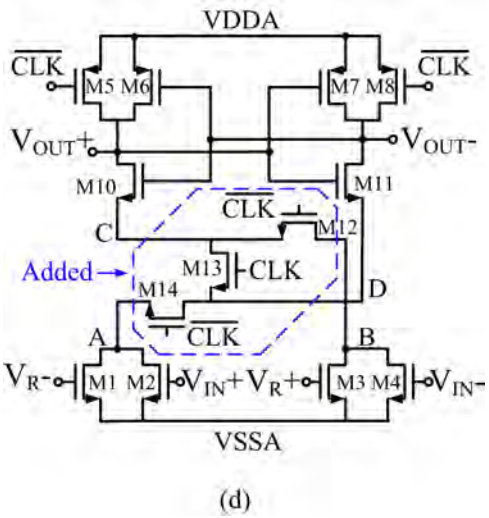


Figure 2 Proposed low offset low kick-back dynamic comparator.

mechanism is triggered as in a conventional dynamic comparator, but since nodes C and D are initially at the same voltage, the offset error is reduced. If this transistor was not used, the nodes C and D could have different voltages when CLK goes down and this would imply higher offset voltage. As a result of this modification, this topology presents lower kick-back effect and offset error than the comparators found in the state-of-the-art, consequently, this effect is less dependent on the process variation.

## 3 | SIMULATIONS

Different simulations have been performed to evaluate both the kick-back effect on input signal of the comparators as well as the voltage offset error. For the simulation of the kick-back effect, the gates of the input transistors (M2 and M4) in the four topologies were connected through 50Ω resistors to $V_{IN}^{+}$ and $V_{IN}^{-}$, respectively. $V_{R}^{+}$ and $V_{R}^{-}$ were connected directly to an ideal voltage source. For a fair comparison, the transistors were sized for $k = 1/1$ and $V_R = 0V$. This means that, according to (3), the theoretical trip point should be placed at $0V$. Fig. 3 shows the results obtained for a typical means condition for the four topologies.

The results show that when a comparison is made, a glitch is created over the input voltage of each dynamic comparator. The peak-to-peak voltage amplitude of each glitch allows the comparison of the kickback noise for each individual topology under test. The simulations of the four topologies show that the proposed circuit has the lowest kickback noise ($287.9\mu V_{pp}$) in an order of magnitude in comparison to CIDC, CDC and LODC. These topologies had a kickback noise of $1342.1\mu V_{pp}$, $2309.4\mu V_{pp}$ and $1567.5\mu V_{pp}$, respectively. On the other hand, CDC presents the higher kick-back effect because of the direct coupling between the output and the input signals through the transistor M10 and M11. CIDC and LODC present similar performances when the kick-back effect is evaluated. Fig. 4 shows a transient simulation of the proposed comparator for four clock semi-cycles.

The simulation was done using a range that covers negative and positive input differential voltage values next to zero. The figure shows that the output of the comparator ($V_{OUT}^{-}$, $V_{OUT}^{+}$) for the negative values is $V_{OUT}^{-} = High$ and $V_{OUT}^{+} = Low$. Subsequently, when the values are positive, $V_{OUT}^{-} = Low$ and $V_{OUT}^{+} = High$, being $High = 3.3V$ and $Low = 0V$. This figure shows the strong coupling that exists between the node A and B with respect to the outputs of the dynamic comparator but this also shows that the distortion over the input signals is drastically minimized. Once the kick-back effect was simulated for the 4 dynamic comparators, offset voltage was evaluated with respect to the technological process variation in order to reach a robust design. Fig. 5 shows the four histograms obtained from the Montecarlo simulations, where the total number of bins were 200.

The histograms show a very low offset voltage variation for CIDC and LODC configurations. The variations of the offset voltage are within the range from -30 $mV$ to 40 $mV$ for CIDC and LODC. On the other hand, CDC presents the highest deviation of the offset error. This deviation varies from -400 $mV$ to 400 $mV$ making its implementation in the pipelined ADC critical. Moreover, another drawback of this topology is the high kick-back effect shown in Fig. 3.a.

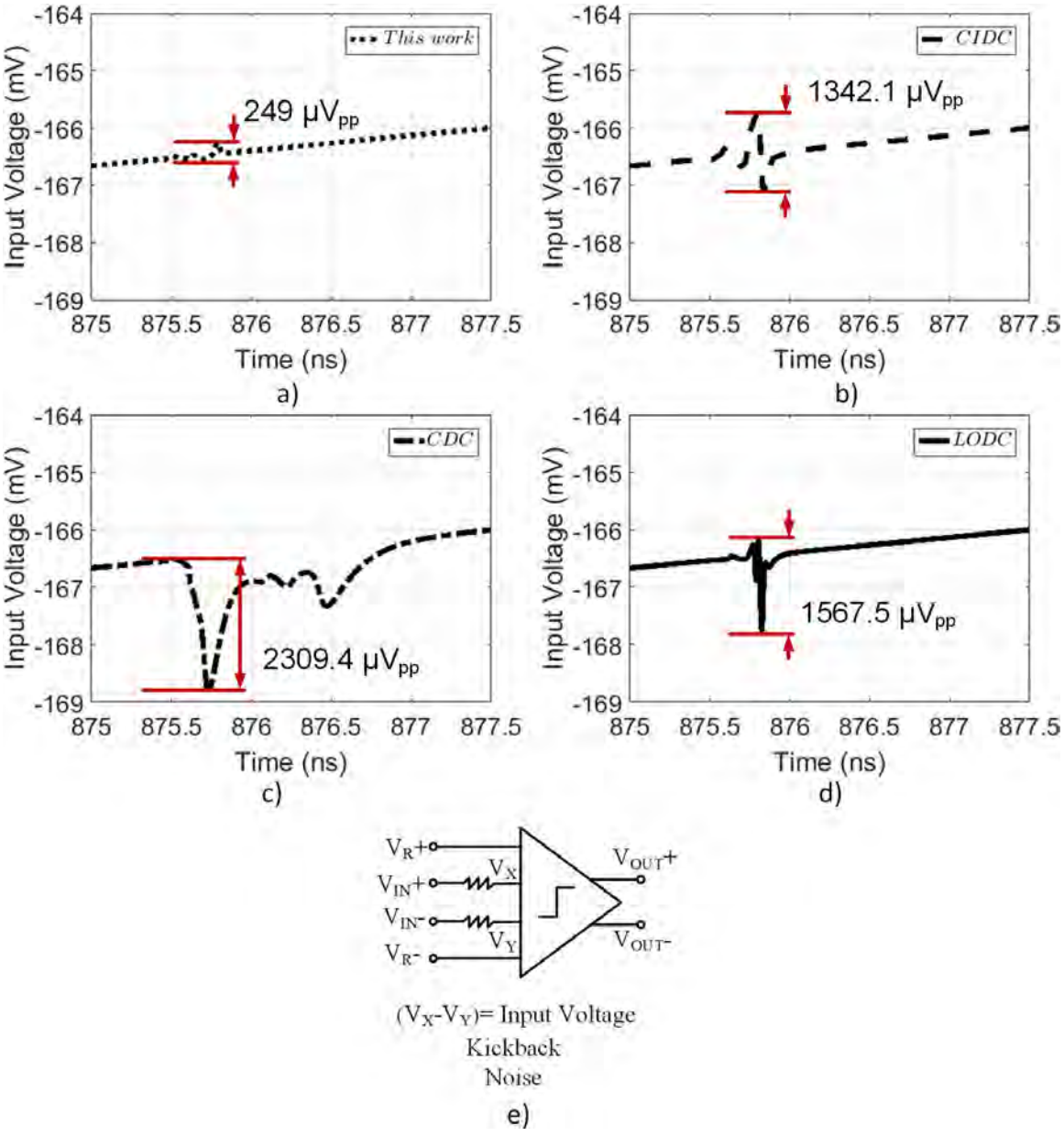


Figure 3 Kickback effect of the four dynamic comparators for k=1: a) This work, b) CIDC, c) CDC, d) LODC and e) Testbench for the measurement of the kickback effect.

On the other hand, the comparator presented in this study has an offset voltage in the range from -250 $mV$ to 200 $mV$. Although the obtained offset voltage is one order of magnitude higher than the measured for CIDC and LODC, this offset voltage allows the fulfillment of the specification for a maximum offset voltage of 375$mV$ defined initially for the pipelined ADC. Diversely, from the point of view of the current specifications of the dynamic comparator and the pipelined ADC, a lower offset voltage in the comparator would not improve the effective resolution the ADC. In contrast, the current magnitude of the kick-back effect over the input signals of the first stages of the pipelined ADC is an important source of distortion which seriously affects the Signal Noise Distortion Ratio (SNDR) of the ADC.

Finally, Fig.6 shows the propagation delay obtained in the four topologies of dynamic comparators under study. The simulations of these circuits show that they have a similar propagation delay around 380$ps$. The obtained propagation delays for this work, CIDC, CDC and LODC were 296.14$ps$, 462.94$ps$, 251.86$ps$ and 353.96$ps$, respectively. The propagation delay was measured with respect to the clock signal with a period of 25$ns$. The results shows that the delay propagation is two orders of

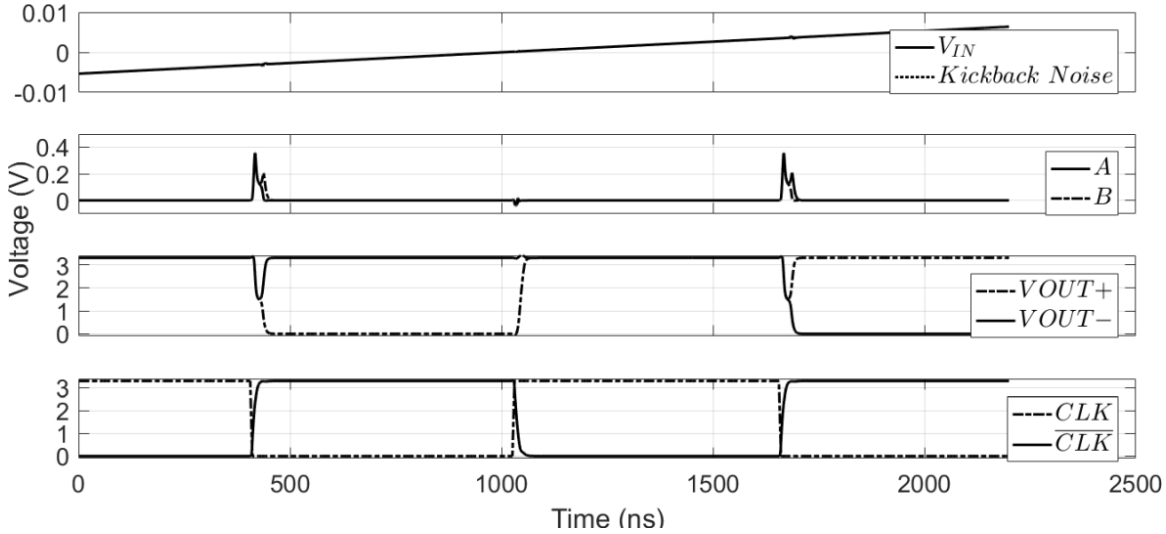


Figure 4 Waveforms of the comparator inputs, outputs and critical nodes of the proposed topology.

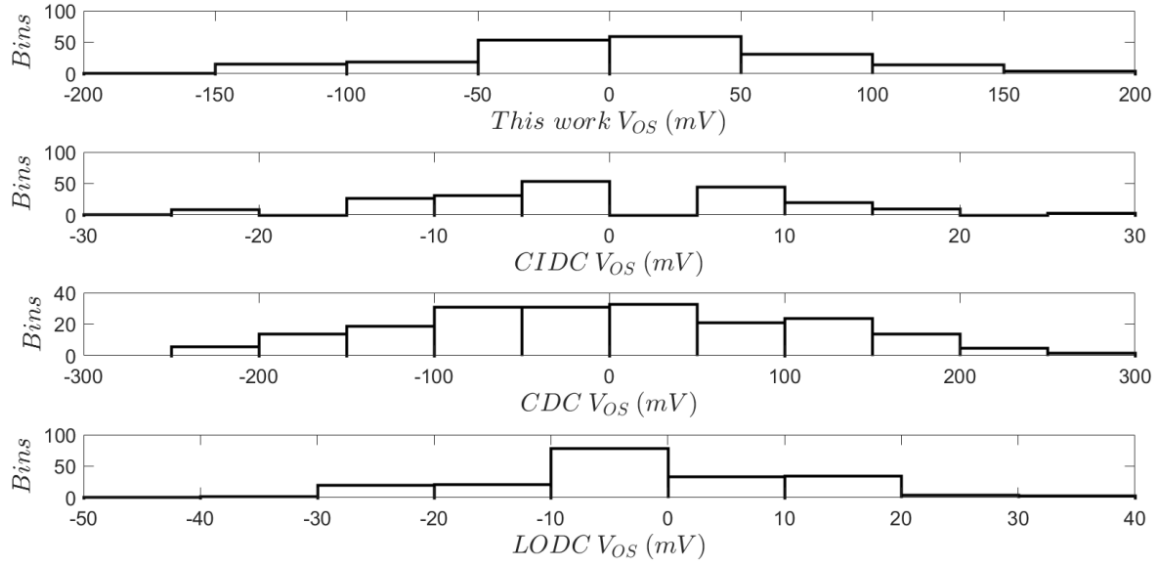


Figure 5 Offset voltage error for Montecarlo process variation the 4 dynamic comparators for $k = 1$.

magnitude smaller than the period of the clock signal. Moreover, another result of the simulation is that the CDC topology and this works present the minimum delay propagation while CIDC show the higher delay. It proves that the influence of the transistors M12 and M14 over the delay propagation is minimal. With respect to the power consumption, since there is no static current, the results show that the differences in power consumption of the topologies under study are negligible. The obtained power consumption for this work, CIDC, CDC and LODC were $70.12\mu W$, $76.82\mu W$, $72.24\mu W$ and $70.75\mu W$, respectively.

Table 1. shows the results, for the proposed comparator, of the eight corner conditions recommended by the AMS foundry. From this analysis, it can be concluded that the offset error of the proposed dynamic comparator does not depend on the corner conditions defined in Table 1. This means that the design is more affected by the process variations and the matching of the transistors than by the corner conditions defined in Table 1. Thus, the comparator shown in this work presents a good trade-off between kick-back effect and offset voltage.

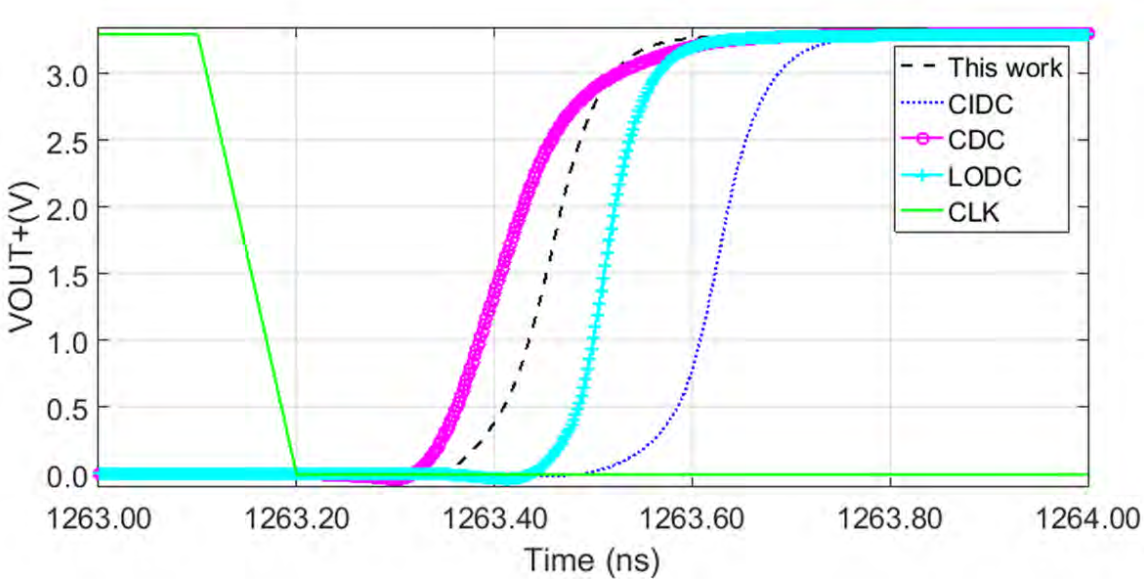


Figure 6 Propagation delay for the four topologies of dynamic comparator under study

Table 1 Summarized offset error for corner simulations for the comparator. TM: Typical mean, WP: Worse Power, WS: Worse Speed, WZ: Worse Zero, WO: Worse One. Austriamicrosystems AG.

| **Corner** | **1** | **2** | **3** | **4** | **5** | **6** | **7** |
|---|---|---|---|---|---|---|---|
| CMOS | WP | WS | WS | WO | WO | WZ | WZ |
| Temp(°C) | 10 | 10 | 45 | 10 | 45 | 10 | 45 |
| VDD [V] | 3.4 | 3.2 | 3.2 | 3.4 | 3.2 | 3.4 | 3.2 |
| $V_{OS,Comp}$ [mV] | 1.3 | 1.3 | 1.3 | 1.3 | 1.3 | 1.3 | 1.3 |

## 4 | EXPERIMENTAL RESULTS

Fig. 7 shows six full differential dynamic comparators and a digital encoder implemented as a low-resolution ADC. At the same time, this circuit is used for the implementation of the stages of an 11-bit pipelined ADC. Moreover, according to this low-resolution ADC, each stage has a resolution $B_i = 3$ and a redundancy $r = 1$ and consequently, each stage has a resolution of 2.5 effective bits. The maximum offset voltage allowed in the comparators for such resolution and redundancy is less than $\pm 375\ mV$. The low-resolution ADC requires configuration for the dynamic comparators with $k = 1/8, 3/8$ and $5/8$. The analog inputs are $V_{IN}^{+}$, $V_{IN}^{-}$, $V_{R}^{+}$ and $V_{R}^{-}$, the digital input is the clock signal $CLK$ and the digital output are $BIT0$, $BIT1$ and $BIT2$. In this circuit, the most significant bit ($MSB$) is $BIT0$ while $BIT2$ is the $LSB$. Therefore, the expected digital outputs are shown in Table 2. This circuit has been synthesized using a 0.35 $\mu m$ CMOS AMS C35B4 process technology.

Fig. 8 shows the micrograph of the prototyped low-resolution ADC. The picture displays 5 of the 6 dynamic comparators. The area occupied by a single comparator is $38x34\ \mu m^2$ while the whole area of the low resolution ADC is $168x310\ \mu m^2$.

Fig. 9 shows the laboratory measurements obtained using a differential ramp input voltage with a frequency of $1.578MHz$ and a clock frequency of $60MHz$. The input reference voltages were internally generated through bandgap circuits and analog buffers. The internal reference voltage $V_R$ was estimated through the real measurements and the lineal regression technique obtaining $V_R = 1.566V$. Table 3 shows the theoretical trip point values, the estimated trip points using $V_R = 1.566V$ and the offset voltage obtained for each dynamic comparator. The measured results show that the dynamic comparators present an offset voltage lower than the maximum offset voltage of $375mV$

Table 2 Expected results for the low resolution ADC

| Input voltage range | BIT0 | BIT1 | BIT2 |
|---|---|---|---|
| $V_{IN} < -5/8 \cdot V_R$ | 0 | 0 | 0 |
| $-5/8 \cdot V_R > V_{IN} < -3/8 \cdot V_R$ | 0 | 0 | 1 |
| $-3/8 \cdot V_R > V_{IN} < -1/8 \cdot V_R$ | 0 | 1 | 0 |
| $-1/8 \cdot V_R > V_{IN} < +1/8 \cdot V_R$ | 0 | 1 | 1 |
| $+1/8 \cdot V_R > V_{IN} < +3/8 \cdot V_R$ | 1 | 0 | 0 |
| $+3/8 \cdot V_R > V_{IN} < +5/8 \cdot V_R$ | 1 | 0 | 1 |
| $V_{IN} > +5/8 \cdot V_R$ | 1 | 1 | 0 |

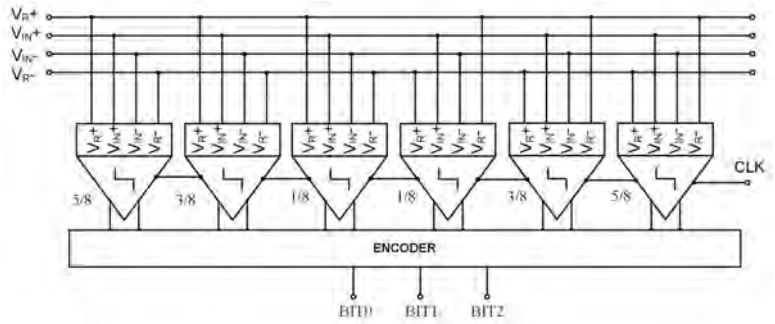


Figure 7 Low resolution ADC of 2.5 effective bit.

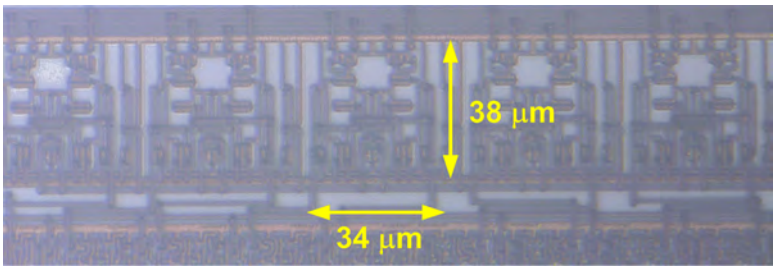


Figure 8 Micrograph of an array of five dynamic comparators.

## 5 | CONCLUSIONS

In this paper, a fully differential dynamic comparator with low kick-back noise has been described. The circuit exhibits a reduction of the kick-back noise at least in one order of magnitude with respect to the other topologies under study and a propagation delay two orders of magnitude smaller than the period of the clock signal, comparable to that achieved by other comparator topologies. The proposed circuit has an offset voltage lower than $\pm 375\ mV$. The circuit comprises a reduced number of transistors, which yields an extremely small silicon area for a 0.35 $\mu m$ CMOS process. Given that the kick-back noise is one of the main factors which limit the resolution of the ADCs and according to the simulations and experimental results presented in this paper, the proposed circuit can be an optimal solution for the design of low power pipeline ADC converters with reduced kick-back noise with stages which effective resolution is less than or equal to 2.5 bits. Moreover, due to the achieved noise reduction, this circuit can be used in other circuits where comparators with a preamplifier stage were required, contributing to a reduction of the power consumption in these circuits.

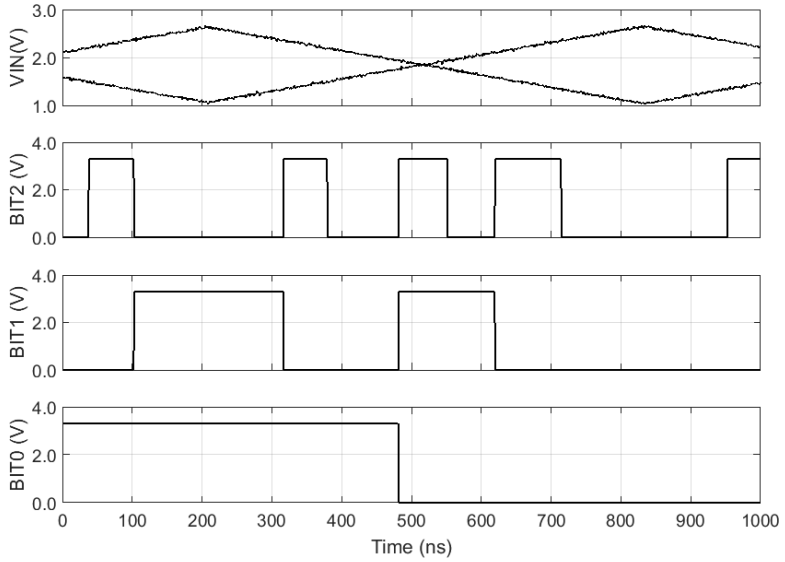


Figure 9 Real measurements for low-resolution ADC of 2.5 effective bit using a differential ramp input voltage with a frequency of $1.578 MHz$

Table 3 Trip points and measured offset voltage in the low-resolution ADC for an internal reference voltage of $V_R = 1.566V$

| **Ideal Trip point** | **Estimated Trip Point** $(V)$ | **Measured Trip Point** $(V)$ | **Offset voltage** $(V)$ |
|---|---|---|---|
| $-5/8 \cdot V_R$ | -0.979 | -1.01 | -0.031 |
| $-3/8 \cdot V_R$ | -0.587 | -0.71 | -0.012 |
| $-1/8 \cdot V_R$ | -0.196 | -0.19 | 0.005 |
| $+1/8 \cdot V_R$ | 0.196 | 0.17 | 0.026 |
| $+3/8 \cdot V_R$ | 0.587 | 0.51 | -0.077 |
| $+5/8 \cdot V_R$ | 0.979 | 1.03 | 0.051 |

## 6 | ACKNOWLEDGEMENTS

This work has been partially funded by Spanish government projects TEC2015-66878-C3-2-R (MINECO/FEDER, UE) and RTI2018-097088-B-C33 (MINECO/FEDER, UE).

## References

1. Yasue, T., et al.: A 33Mpixel CMOS imager with multi-functional 3-stage pipeline ADC for 480 fps high-speed mode and 120 fps low-noise mode, Proc. of the IEEE International Solid-State Circuits Conference. 90-92, (2018)

2. Yazid, M.: Low-noise dynamic comparator circuit with selectable input-referred thermal noise voltage, Electronics Letters, 54, 1210-1212, (2018)

3. Figueiredo, P.M., Vital, J.C.: Kickback noise reduction techniques for CMOS latched comparators, IEEE Trans. Circuits Syst. II Express Briefs., 2006, 53, 541-545, (2006)

4. Duong, D. V., Nguyen, T. V.: A capacitive dynamic comparator with low kickback noise for pipelined ADC, IEEE International Conference on Electronics, Computing and Communication Technologies, Bangalore, 2013, pp. 1-4. doi: 10.1109/CONECCT.2013.6469281, (2013)

5. Yongzhen, C., Chixiao, C., Zemin, F., Fan, Ye., Junyan, R.: 14-bit 100 MS/s 121 mW pipelined ADC, Journal of Semiconductors, 36, 065008-1–065008-6, (2015)

6. Bahmanyar, P., Maymandi-Nejad, M., Hosseini-Khayat, S., Berekovic, M.: Design and analysis of an ultra-low-power double-tail latched comparator for biomedical applications, Analog Integr Circ Sig Process, 86, 159–169, (2016)

7. Ayesh, M. Ibrahim, S., Aboudina, M.M.: Design and Analysis of a Low-Power High-Speed Charge-Steering Based StrongARM Comparator, 28th International Conference on Microelectronics (ICM), Giza, 209-212, (2016)

8. Khorami, A., Sharifkhani, M. : A high-speed method of dynamic comparators for SAR analog to digital converters, IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), Abu Dhabi, 1-4, (2016)

9. Rusli, J. R., Sidek, R. M., Majid, H. A., Hassand, W. Z. W., Mustafa, M. A., Shafie, S.: Design and Verification of Low Voltage Low Power Dynamic Comparator over PVT Variation, IEEE 5th International Conference on Smart Instrumentation, Measurement and Application (ICSIMA), Songkla, Thailand, 1-5, (2018)

10. Mahdavi, S., Poreh, M., Ataei, S., Jafarzadeh, M., Noruzpur, F.: A New 1 GS/s Sampling Rate and 400 V Resolution with Reliable Power Consumption Dynamic Latched Type Comparator. In: Montaser Kouhsari S. (eds) Fundamental Research in Electrical Engineering. Lecture Notes in Electrical Engineering, vol 480. Springer, Singapore, (2019)

11. Cho, T.B., Gray, P.R.: A 10 b, 20 Msample/s, 35 mW pipeline A/D converter, IEEE Journal of Solid-State Circuits, 30, 166-172, (1995)

12. Lee, S.M., et al: Enhanced input range dynamic comparator for pipeline analogue-to-digital converter, Electronics Letters, 45, 728-730, (2009)

13. Min, B.M., Kim, P., Bowman, F., W., Boisvert D.M., Aude A.J.: A 69-mW 10-bit 80-MSample/s Pipelined CMOS ADC, IEEE Journal of Solid-State Circuits, 38, 2031-2039, (2003)