

# The control unit of the near infrared spectrograph of the Euclid space mission: detailed design

Rafael Toledo-Moreo<sup>a</sup>, Carlos Colodro-Conde<sup>a</sup>, Jaime Gómez-Sáenz-de-Tejada<sup>a</sup>, David Pérez-Lizán<sup>a</sup>, José Javier Díaz-García<sup>b</sup>, Oscar Tubío-Araujo<sup>b</sup>, Cayetano Raichs<sup>c</sup>, Jordi Catalán<sup>c</sup>, and Rafael Rebolo-López<sup>b</sup>

<sup>a</sup>Univ. Politécnica de Cartagena, Spain

<sup>b</sup>Instituto de Astrofísica de Canarias, Spain

<sup>c</sup>Crisa, an Airbus Defence and Space Co., Spain

## ABSTRACT

The Near Infrared Spectrograph and Photometer (NISP) is one of the instruments on board the ESA EUCLID mission. The Universidad Politécnica de Cartagena and Instituto de Astrofísica de Canarias are responsible of the Instrument Control Unit of the NISP (NI-ICU) in the Euclid Consortium. The NI-ICU hardware is developed by CRISA (Airbus Defence and Space), and its main functions are: communication with the S/C and the Data Processing Unit, control of the Filter and Grism Wheels, control of the Calibration Unit and thermal control of the instrument. This paper presents the NI-ICU status of definition and design at the end of the detailed design phase.

**Keywords:** Control electronics, space instrumentation, spectro-photometer

## 1. INTRODUCTION

Euclid is the Medium Class mission of the ESA Cosmic Vision 2015-2025 programme selected in 2011, with a foreseen launch slot in 2020. The main objective of Euclid<sup>1,2</sup> is to understand the origin of the accelerating expansion of the Universe by studying the dark matter and the dark energy.

The Euclid spacecraft is equipped with a 1.2 m Korsch telescope, which directs the light to two instruments: the visual instrument<sup>3</sup> (VIS) and the near infrared instrument<sup>4</sup> (NISP). With these instruments physicists will probe the expansion history of the Universe and the evolution of cosmic structures by measuring the modification of shapes of galaxies induced by gravitational lensing effects of dark matter and the 3-dimension distribution of structures from spectroscopic redshifts of galaxies and clusters of galaxies.<sup>5</sup>

The NISP instrument performs imaging photometry and slitless spectroscopy measurements in sequence inserting optical components in the light path by configuring a filter wheel<sup>6</sup> (NI-FWA) and a grism wheel<sup>7</sup> (NI-GWA). Besides the wheel cryomechanisms, the mechanical structure of the instrument (NI-OMADA, Opto-Mechanical Assembly and Detector Assembly) encompasses the Calibration Unit (NI-CU) and the Focal Plane Array<sup>8</sup> (NI-FPA). The process of acquiring and processing the science data is handled by the Data Processing Unit<sup>9</sup> (NI-DPU), while the overall control of the instrument is done by another piece of electronics: the Instrument Control Unit<sup>10</sup> (NI-ICU).

Among all the institutions participating in this mission, the Universidad Politécnica de Cartagena (UPCT), in collaboration with the Instituto de Astrofísica de Canarias (IAC) and with a contract with CRISA (Airbus Defence and Space), is responsible for the design, manufacturing and validation of the control electronics of the NISP instrument, that is, the NI-ICU.

This paper presents the NI-ICU status of definition and design at the end of the detailed design phase. The structure of the paper is as follows: Section 2 explains the functions that the NI-ICU shall provide. Section 3 describes the internal architecture of the NI-ICU at the current stage of development. Then, Section 4 briefly presents the mechanical interface. Lastly, Section 5 describes the current NI-ICU test environment.

---

Rafael Toledo-Moreo: E-mail: rafael.toledo@upct.es, Telephone: +34 968 32 59 48

## 2. FUNCTIONAL DESCRIPTION

The NI-ICU handles all the NISP functionalities, and interfaces the NISP instrument to the S/C control system for TM&TC tasks. It exchanges TM&TC data with the NI-DPU using a dedicated intra-instrument interface. It provides the control electronics for the NI-FWA, the NI-GWA and the NI-CU. It is also responsible for the monitoring of the NI-OMADA temperature sensors and powering the heaters, and it maintains HK data of the NISP warm electronics (NI-WE). The NI-ICU generates the secondary power supplies which are needed to perform all these functions except from the DPU-DCU, whose main power supply and secondary power needs are self-provided.

The NI-ICU will be constituted by two identical sections, one nominal, the other in cold redundancy. Both nominal and redundant sections will be installed in a single box with verified structural and thermal conditions. No kind of cross-redundancy is foreseen for external elements under NI-ICU control (heaters, sensors, LEDs, etc); meaning that nominal elements will be connected to the nominal NI-ICU and redundant elements will be connected to the redundant NI-ICU. This implies that the nominal NI-ICU can only control nominal elements and that the redundant NI-ICU can only control redundant elements. An exception to this is the interface with the DPU, whose baseline now is to have 4 CPU boards in warm redundancy. In this last case, both N+R ICU sections must interface all 4 DPU boards.

## 3. DESCRIPTION OF THE ARCHITECTURE

Internally, each section of the NI-ICU (nominal or redundant) is organized in four boards:

- The LVPS (Low Voltage Power Supply) takes the 28V power line from the S/C primary bus and produces all the necessary secondary power supplies by means of DC/DC converters. These secondary lines are used to power the NI-OMADA elements under NI-ICU control, as well as the NI-ICU electronics themselves. The LVPS board allocates the EMC filters so as to meet the electromagnetic compatibility requirements. Finally, a non-power-related feature is also provided by this board: the intra-instrument MIL-STD-1553B<sup>11</sup> transceivers, which do not fit in the CDPU board because of PCB size restrictions.
- The CDPU (Central Data Processing Unit) board is based on Crisa's General Purpose Module (GPM). It features a MDPA ASIC (TRL-9) which includes, among others, a 80MHz LEON2-FT microprocessor, two 1553 interfaces (one used for communications with S/C in RT mode and another one for communications with NI-DPU in BC mode) and several SpaceWire<sup>12,13</sup> interfaces (though the NI-ICU only uses one of them). Regarding memory resources, the board provides 64 KBytes of PROM, 4 MBytes of EEPROM and 8 MBytes of EDAC-protected SRAM. In addition, the CDPU board includes an RTAX2000S1 FPGA which provides functions mainly related to the processor system and internal/external interfaces (e.g., communication with the DAS module).
- The DAS (Driver and Acquisition Support) board, featuring a SECOIA (Serial Control Interface) ASIC (TRL-8) that controls all the driving and acquisition electronics that allow the NI-ICU to interface the NI-OMADA elements under its control, namely:
  - 2 motor coils for each of the two stepper motors of the cryo-mechanism (NI-FWA and NI-GWA).
  - 1 reference position sensor for each wheel.
  - 1 heater in the structure assembly (NI-SA), where the filters and grisms are allocated.
  - 1 heater in the focal plane array of the detectors (NI-FPA).
  - 5 LEDs of the calibration unit, controlled by means of a PWM.
  - 12 PT-100 temperature sensors distributed around the NI-OMADA.

Additionally, the DAS board also acquires NI-ICU internal telemetry such as temperature, voltage and intensity readings.

- All boards are connected between them through a backplane motherboard, which will route the necessary signal and power lines.

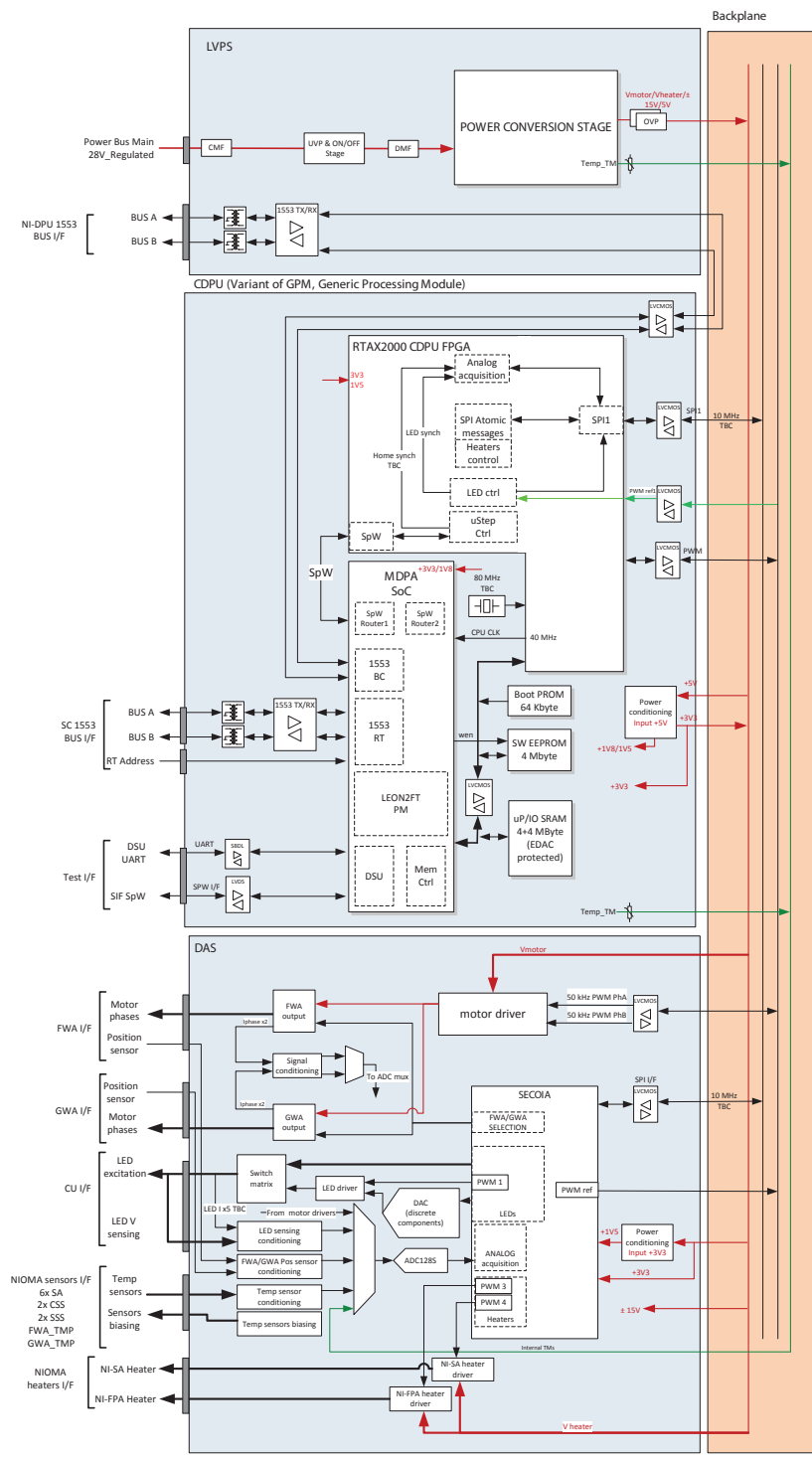


Figure 1. NI-ICU internal architecture.

Fig. 1 illustrates the internal architecture of the NI-ICU. The following subsections will give more detail of the main modules and functions that are depicted in this diagram.

### 3.1 LVPS board

The LVPS module is based on standard DC/DC converters with flyback topology.

There are two DC/DC converters in this module. On one hand, the *Service Converter* generates all the required voltages which the internal electronics (digital and analog) needs. On the other hand, the *Application Converter* is in charge of generating power supplies for the external subsystems such as heaters, motors, clutch, etc.

The first stage just after the primary bus input connector is a filter stage composed of a common and a differential filter. The main goal of the input stage is to filter the noise injected by the converters to the primary bus. Additionally, this filter stage avoids the propagation of any external common or differential EMC perturbation to the internal NI-ICU electronics. That is, it performs a two-way filtering function. This filter stage is shared by the two DC/DC converters.

The DC/DC converters run freely at frequencies about 120-130 kHz, which means that the clock generator is generated by its own internal oscillator and this clock is not synchronised with any other external clock. Therefore, the switching frequency of these converters is a mid-range frequency (one or two hundreds of kHz), which is a good commitment between the reduction of the switching power losses in the power semiconductors and the size got for the magnetic parts.

### 3.2 CDPU board

The CDPU module is based on the Generic Processing (GPM), a standard flight CPU board designed at CRISA-Airbus. Its processing core consists on a 32-bit LEON2-FT microprocessor running at 80 MHz, providing at least 60 MIPS and 15 MFLOPS. The processor is embedded in a MDPA System-on-Chip, designed by Astrium and Manufactured by Atmel. The main features of the MPDA device are as follows:

- SparcV8 (LEON2FT) based processor plus a IEEE-754 FPU.
- 8 SpW interfaces able to operate up to 200 Mbps.
- Two Milbus interfaces configured in BC/BC or BC/RT modes.
- GPIOs and memory interfaces.
- DSU and SIF test interfaces.
- Technology: Atmel ATC18RHA.
- Package: MQFP352.
- Radiation Tolerance: > 300 Krad.
- Latch-up immune for > 70 MeV.cm/mg.
- SEU hardness of 30 MeV.cm<sup>2</sup>/mg for all registers.

The two MIL-STD-1553B links implemented on the MPDA ASIC are based on Airbus standard cores with flight heritage (Alphasat platform). In the NI-ICU, one will operate as a Remote Terminal (S/C side) and the other as a Bus Controller (DPUs side). The GPM itself provides a Remote Terminal MIL-STD-1553B bus interface (controller, transceivers) supporting two physical media (A & B) as well as an external connector for configuring the RT address. The GPM supports an additional MIL-STD-1553B Bus Controller, although the transceiver for this link is not implemented on this board. Instead, the bus signals are available on the CDPU module's motherboard connector, making feasible to place this transceiver on another module. This is the case on NI-ICU, where the transceiver will be mounted on the LVPS module.

Besides the MDPA ASIC, the other main component of the CDPU board is the CDPU FPGA, which contains functions mainly related to the processor system and the internal/external interfaces. The selected device is a RTAX2000S1, a radiation-tolerant FPGA with a large space heritage. The CDPU FPGA implements the following functions:

- MDPA interface: Provides a slave interface to communicate with the MDPA ASIC.

- Memory control signals: Provides decoding logic for the CDPU memories.
- OBT: Provides a local On Board Timer.
- Auxiliary oscillator: Provides a clock input to feed the local OBT with a dedicated  $2^{24}$  Hz clock.
- SPI interface: Provides a master interface to send read and write commands to other boards.
- Motors interface: Allows setting the phase currents of the FWA or GWA motors.
- LEDs interface: Allows configuring the current and duty cycle of the calibration LEDs of the NI-CU.
- TM Acquisition: Provides functionality for automated telemetry acquisition from the DAS board.
- SPI Atomic: Allows accessing the SPI interface for ordering discrete SPI transmissions.

The MDPA accesses all the functions of the CDPU FPGA by means of its memory mapped I/O interface. The only exception is the sending of the motor profile tables, which is done through a dedicated 10 Mbps SpaceWire link that interconnects both devices.

Regarding memory, the CDPU board provides 64 KBytes of PROM arranged in two 32 Kbytes devices, which will be used to store the boot software (BSW) of the NI-ICU. No EDAC protection is implemented on this memory. On the other hand, the 4 MBytes of in-flight rewritable non-volatile EEPROM will be used for storing the application software (ASW) images and configuration/data to be recovered between resets/power cycles (e.g., motor profile tables). Finally, the CDPU module provides 8 Mbytes of SRAM EDAC protected volatile memory to store the ASW code, data buffers, etc., and I/O memory (for data exchange over 1553, etc.). The EDAC en/decoder is implemented by a dedicated hardware module inside the MDPA. The data throughput for accesses from/to the microprocessor to/from the volatile memory will be as minimum 60 MByte/s.

### 3.3 DAS board

The driving and acquisition electronics contained in the DAS board are controlled by the SECOIA ASIC. Among all the functionalities provided by this ASIC, the NI-ICU uses the following ones:

- Communication verification. All accesses to SECOIA registers are protected by parity.
- External ADC control capability with up to 3072 addresses external multiplexing.
- Up to 110 bi-level output signals.
- Capability of define *blocking groups* of bi-level signals. A *blocking group* is a user defined group of signals. The SECOIA ASIC guarantee that only one signal in a blocking group is active. (i.e., if the SECOIA is commanded to activate a more than one signal in a blocking group, the command is discarded).
- 16 PWM generators with the following characteristics:
  - Main frequency is the ASIC frequency (set to 10 MHz).
  - Two independent set of prescalers allows dividing de ASIC Main Clock to three different divisions of MC (tick signals). Each PWM can be configured to use any of the divided MC frequencies.
  - 10 bits PWM (i.e. 1024 steps available).
  - All PWMs using the same clock source are synchronous, and the rise of the activation is configurable.

The CPDU board communicates with the DAS board in order to control the NISP instrument and acquire telemetry and housekeeping parameters. This communication channel consists on a 10 Mbps SPI link between the CDPU-FPGA (which acts as the SPI master) and the SECOIA ASIC in the DAS module (which acts as a SPI slave). Besides the SPI link, there are two PWM lines that are generated by the CDPU FPGA (not by the SECOIA) in order to set the motor driver currents.

#### 3.3.1 Heater driver

The DAS module has two independent heater drivers able to power the NI-SA and NI-FPA heaters. The NI-ICU does not take care of thermal stability by any means. It just applies the specified heating power.

Both drivers have the so-called *control range* where the heater work for controlling thermal gradients of the instrument. In this range, the heater driver will provide the best stability and resolution performances. The

control range is 0 to 4 watts for the NI-SA heater and 0 to 2 watts for the NI-FPA heater. Above the control range, both heaters will implement the *decontamination* zone, where the heaters will be used for maintenance purposes. In this zone, the heater drivers will provide reduced resolution and stability since the decontamination is a less demanding functionality from the performance point of view. The decontamination range for the NI-SA heater goes from 4 up to 10 watts. The NI-FPA heater requires from 2 to 6 watts for this maintenance process.

The heater driver concept on the NI-ICU is a programmable voltage regulator. A hardware control loop is in charge of keeping stable the voltage provided to the heater. The output voltage of the regulator can be modified by changing its reference signal. The reference signal is generated as a PWM signal which is output by the SECOIA and filtered by a low-pass filter to obtain a DC signal. This mechanism allows obtaining an accurate analogue reference signal from a digital basis.

The solution leads to a controlled voltage on the load (heater). Any drift on the load will be transparent to the driver which will continue applying the programmed voltage. Therefore, a drift on the heater resistance will lead to a different power level on the load.

### 3.3.2 Motor drivers

The NI-FWA and NI-GWA are two rotating wheels used to position filters and grisms as required by the NISP observing and calibration sequences. All the movements required are determined in advance. Each movement is defined by a *Motion Profile* containing the rotation angle vs time information to produce an acceleration controlled rotation.

The current profiles that determine the FWA and GWA motor movements are stored in EEPROM memory on the CDPU board. The ASW is in charge on loading these profiles into the CDPU RAM and then send them to the CDPU FPGA through the SpaceWire link. Then, the CDPU FPGA generates the PWM signals that execute the received microstepping profile at the right timing. These signals are routed through the backplane motherboard, and they determine the amount of current that the motor driver on the DAS board inject into the motor coils by means of a PWM-controlled current source.

The DAS board implements just one motor driver. The output of this single motor driver is connected to the FWA or GWA motor by means of two SECOIA bilevel signals, and three SECOIA bi-level signals are used to activate/deactivate motor driver.

The motor driver itself consists of two H-bridges each of them with four MOSFET and the corresponding drivers, in order to drive motor windings in bipolar mode (the H-bridge can be configured to allow the current to flow in either direction across the winding). Freewheeling diodes will be implemented with the MOSFET built in ones. To minimize the EMI in the harness between the driver and the motor two low pass LC filter have been inserted across the outputs of the H-bridge. The motor current is sensed at the output between both EMI filter stages. Therefore, the noise induced by the bridge switching is reduced to the minimum.

After initialization, or when it is required, the NI-ICU shall be able to set the NI-FWA or NI-GWA in a predetermined position, called the *home position*. For this purpose, both wheel assemblies include a reference position sensor, implemented as a variable differential transformer (LVDT) with one excitation coil in the stator and two measurement coils in the rotor. The amplitude at the outputs of the LVDT are thresholded with a configurable comparator and stored in two latches. Then, the SECOIA acquires these digital signals using two of its bilevel acquisition channels, thus making them available to the ASW on request. The ASW can know if the wheel has crossed the reference position by acquiring these digital signals after the completion of each motor step and later analysing them. Fig. 2 shows the circuitry in the DAS board that is used to read the home position sensor as explained in this paragraph.

### 3.3.3 Calibration unit controller

The calibration unit controller on the NI-ICU implements electronics to excite the five external calibration LEDs on the NI-CU subsystem. The NI-CU provides direct illumination of the NISP focal plane in order to allow small-scale flatfield calibration as well as linearity measurements of the detector. It will contain 5 nominal LEDs plus 5 redundant ones. The five nominal will be controlled by the nominal NI-ICU and the five redundant LEDs will be controlled from the redundant NI-ICU. Each LED has 4 wires, 2 for driving and 2 for sensing.

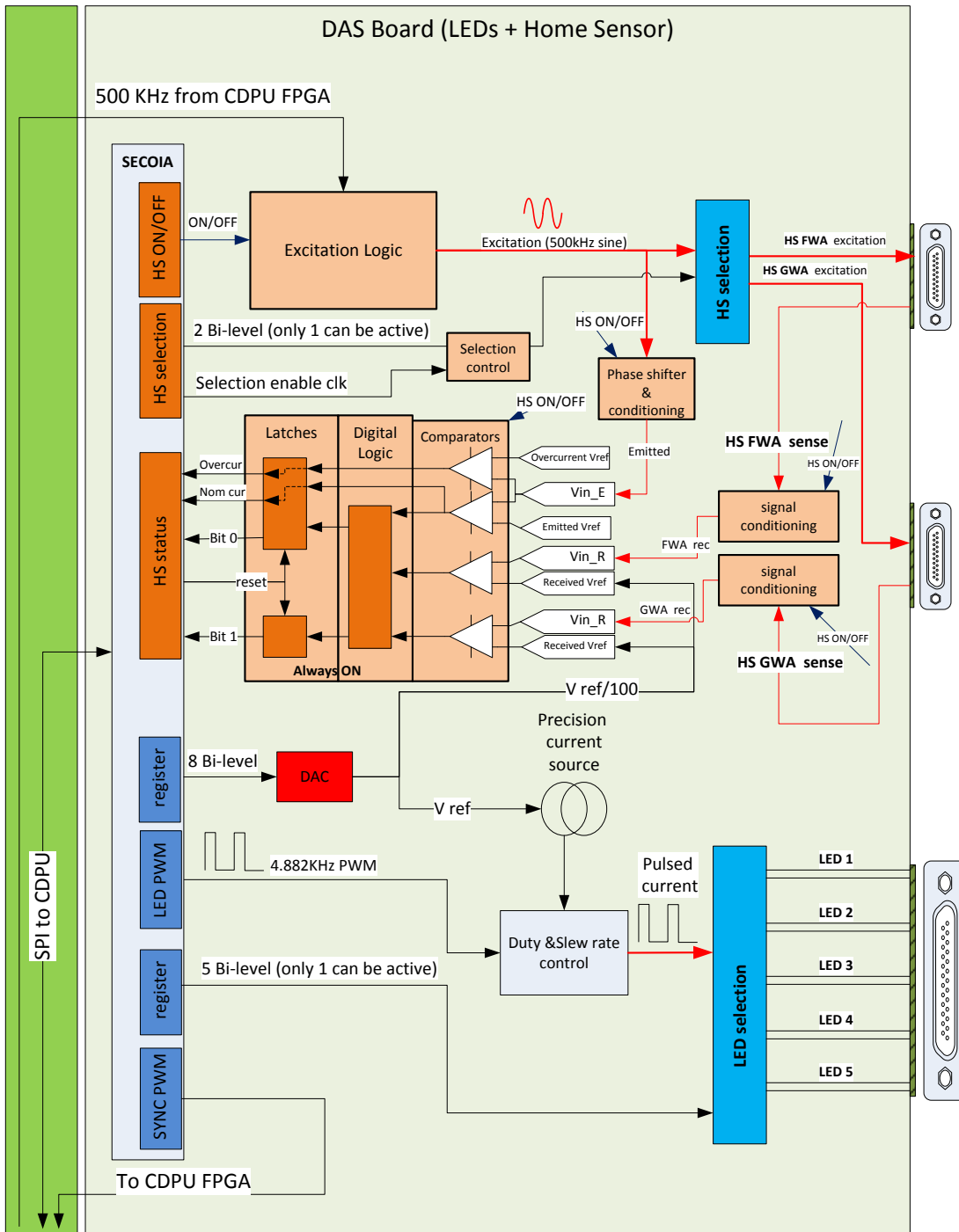


Figure 2. DAS board: home sensor and LED electronics.

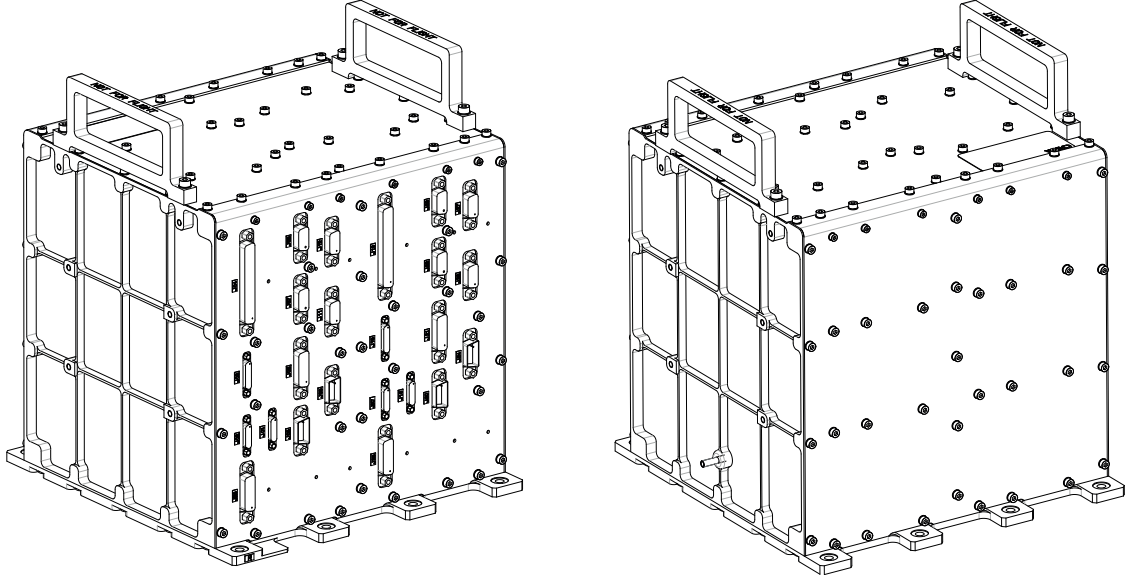


Figure 3. NI-ICU mechanical interface drawing.

As shown in Fig. 2, the output of the LED driver is connected to one of the calibration LEDs by means of a switch matrix controlled by five SECOIA bilevel signals. One SECOIA bilevel signal blocking group is used to guarantee that at most one LED is connected to the LED driver. Eight SECOIA bi-level signals are used for selecting the value in the DAC that establishes the amount of current injected by the LED current source. A SECOIA PWM channel is used to pulse the current at 4882 Hz, with the duty cycle configurable in 1024 steps.

### 3.3.4 Analogue acquisition chain

The DAS module implements a analogue acquisition chain in charge of converting different analogue signals distributed along the instrument and inside the NI-ICU itself, including the 12 PT-100 sensors distributed along the NI-OMADA, the temperature sensors that measure the temperature of the CPDU and LVPS boards, the NI-CU DAC reference voltage, the internal 3.3V voltage, the driving voltages of the NI-CU LEDs, NI-FWA/NI-GWA coils, NI-SA heater, NI-FPGA heater, etc.

The analogue acquisition chain is based on the well-known 12-bit converter ADC128S from National Semiconductor. This device has 8 input channels but the NI-ICU needs to acquire more than 8 analogue channels, so additional analogue multiplexers are included in the DAS design. The SECOIA will be in charge of controlling both ADC itself and the surrounding analogue multiplexers, just as requested by the ASW running on the CPDU board.

For reading the temperature of the PT100 sensors, the sensors are driven with moderate current to avoid self-heating issues. The measurement will be performed using the common 4-wire topology, which avoids harness voltage drops.

## 4. PHYSICAL ARCHITECTURE

The NI-ICU unit will be assembled as a vertical stack of six modules that are three nominal and three redundant and have a very similar structure. These six modules are stacked in a vertical position over a baseplate and be enclosed by three flat plates (left cover, right cover and mother board cover) forming so an EMC enclosure. In this stacking, modules are fixed together by a set of long screws that cross lateral covers and modules through machined holes from one side to the opposite and they are fixed with washers and nuts. The connectors for interfacing are all on the same face of the unit. Therefore, for flight configuration, all the connectors will be available on the same side. Fig. 3 shows a drawing of the mechanical interface that illustrates this description.





Figure 4. Elegant Bread-Board 3 (EBB3)

The unit width is a direct consequence of the addition of the assembled modules pitch and the thickness of lateral covers, thus empty volume is minimized as well as mechanical parts, in order to reduce mass budget to a minimum.

## 5. TEST ENVIRONMENT

The current test environment available at UPCT is built around piece of hardware called EBB3 (Elegant Bread-Board 3), whose picture is shown in Fig. 4. The EBB3 is a flight-representative model of the CDPU board of the NI-ICU that does not use space-level electronic components. It includes a proto (i.e., non-flight) MPDA ASIC and a Microsemi ProASIC3 FPGA for simulating the RTAX2000 of the actual NI-ICU. The ProASIC3 is plugged into a socket that has the same PCB footprint as the RTAX2000. Another difference with the flight NI-ICU model is that EBB3 does not have PROM memories, but flash memories.

There is no simulator of the LVPS board at this stage of the project. The EBB3 is just powered with a commercial power supply. The MIL-STD-1553B transceivers for the intra-instrument interface are implemented in an auxiliary board inside the EBB3 itself. In Fig. 4, the connectors can be seen on the top row of the EBB3 assembly.

The EBB3 relies on an external auxiliary board called the *Setup Board*. This board adapts the voltage levels from the commercial power supply, adapts the DSU serial line of the CDPU LEON from RS422 to RS232 and provides a Spartan-3 FPGA that can be programmed to simulate the SPI responses of the SECOIA of the actual DAS board, as if it was connected to the NISP instrument. This behaviour will be specially useful during the development and testing of the ASW, as well as for the validation of the software drivers that interact with the rest of elements of the NISP instrument.

## ACKNOWLEDGMENTS

The authors want to acknowledge the contributions provided by the NISP system team of the Euclid Consortium to this work. This work has been supported by the Spanish Ministry of Economy under the projects ESP2013-48362-C2-2-P, ESP2014-56869-C2-2-P and ESP2015-69020-C2-2-R, as well as by ERDF funds from the European Commission.

## REFERENCES

- [1] Laureijs, R. J., Duvet, L., Escudero Sanz, I., Gondoin, P., Lumb, D. H., Oosterbroek, T., and Saavedra Criado, G., “The Euclid Mission,” in [*Space Telescopes and Instrumentation 2010: Optical, Infrared, and Millimeter Wave*], Proc. SPIE **7731**, 77311H (July 2010).
- [2] Laureijs, R., Racca, G., Stagnaro, L., Salvignol, J.-C., Lorenzo Alvarez, et al, “Euclid mission status,” in [*Space Telescopes and Instrumentation 2014: Optical, Infrared, and Millimeter Wave*], Proc. SPIE **9143**, 91430H (Aug. 2014).
- [3] Cropper, M., Pottinger, S., Niemi, S.-M., Denniston, J., Cole, R., et al, “VIS: the visible imager for Euclid,” in [*Space Telescopes and Instrumentation 2014: Optical, Infrared, and Millimeter Wave*], Proc. SPIE **9143**, 91430J (Aug. 2014).
- [4] Maciaszek, T., Ealet, A., Jahnke, K., Prieto, E., Barbier, R., et al, “Euclid near infrared spectrophotometer instrument concept and first test results at the end of phase B,” in [*Space Telescopes and Instrumentation 2014: Optical, Infrared, and Millimeter Wave*], Proc. SPIE **9143**, 91430K (Aug. 2014).
- [5] Euclid Consortium, “Euclid Consortium - A space mission to map the Dark Universe”. <http://www.euclid-ec.org/>, accessed 13-05-2014.
- [6] Holmes, R., Grözinger, U., Krause, O., and Schweitzer, M., “A filter wheel mechanism for the Euclid near-infrared imaging photometer,” in [*Modern Technologies in Space- and Ground-based Telescopes and Instrumentation*], Proc. SPIE **7739**, 77391A (July 2010).
- [7] Riva, M., Barriere, J.-C., Ferrand, D., Maciaszek, T., Prieto, E., Valenziano, L., and Zerbi, F. M., “Euclid NISP GWA and compensating mechanism,” in [*Space Telescopes and Instrumentation 2012: Optical, Infrared, and Millimeter Wave*], Proc. SPIE **8442**, 844211 (Sept. 2012).
- [8] Clémens, J. C., Serra, B., Niclas, M., Ealet, A., Gillard, W., et al., “EUCLID detector system demonstrator model: a first demonstration of the NISP detection system,” in [*Optics for EUV, X-Ray, and Gamma-Ray Astronomy VII*], Proc. SPIE **9602**, 96020Y (Sept. 2015).
- [9] Corcione, L., Ligorì, S., Capobianco, V., Bortoletto, F., Bonoli, C., D’Alessandro, M., Longoni, A., Grimoldi, R., and Valenziano, L., “The data processing unit of the NISP instrument of the Euclid mission,” in [*Space Telescopes and Instrumentation 2014: Optical, Infrared, and Millimeter Wave*], Proc. SPIE **9143**, 914331 (Aug. 2014).
- [10] Toledo-Moreo, R., Colodro-Conde, C., Díaz-García, J. J., Tubío-Araujo, Ó. M., Gómez-Sáenz, J., Peña-Godino, A., Velasco-Fernández, T., Sánchez-Prieto, S., Villó-Pérez, I., and Rebolo-López, R., “The control unit of the near infrared spectrograph of the EUCLID space mission: preliminary design,” in [*Space Telescopes and Instrumentation 2014: Optical, Infrared, and Millimeter Wave*], Proc. SPIE **9143**, 91432W (Aug. 2014).
- [11] ECSS “Space engineering: Interface and communication protocol for MIL-STD-1553B data bus onboard spacecraft.” Standard ECSS-E-50-13C, ESA Requirements and Standards Division (2008).
- [12] ECSS, “Space engineering: SpaceWire - Links, nodes, routers and networks.” Standard ECSS-E-ST-50-12C, ESA Requirements and Standards Division (2008).
- [13] Steve Parkes, “SpaceWire User’s Guide”, STAR-Dundee Limited, (2012).