Design Considerations for Single-Stage, Input-Current Shapers for Low Output Voltage Ripple

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Abstract: A lot of power topologies have been proposed to comply with the IEC-61000-3-2 regulations. One group of solutions involves obtaining an additional output from one of the converter's magnetic devices. These solutions are very good due to the low harmonic content and from the low cost point of view. Nevertheless these magnetic coupled circuits can modify the converter's performance. The abnormal operation can be observed as an output voltage ripple higher than expected. This paper deals with the design considerations for low output voltage ripple Single-Stage-Input-Current Shapers (S^2ICS) and explains the abnormalities.

1. INTRODUCTION

Many power topologies have been proposed in order to comply with the IEC 61000-3-2 regulations. Some of them are based on the idea of using standard topologies with small modifications. One possible implementation for this idea is to introduce a "High Impedance Network" (HIN) between the input rectifier and the dc-to-dc convert's bulk capacitor (as Fig. 1 shows). This HIN usually is one additional output from one of the converter's magnetic devices (e.g. the main converter transformer). The output impedance of this additional output must be high in order to allow the input rectifier diodes to conduct for a relatively wide conduction angle θ_c. Many active input current shapers [1-6] have been proposed in this way to avoid the traditional drawback of poor dynamic output voltage regulation thanks to its fast voltage control loop and, at the same time, keeping limited voltage boosting in the bulk capacitor.

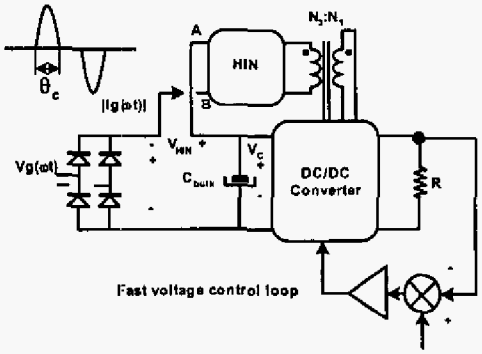

Fig. 1. General scheme of the ac-to-dc converter with HIN

However, the attention has been focused on the input current shape, then another important parameter has been neglected. The additional output of some topologies can interchange energy from the bulk capacitor to the dc-to-dc converter's output. The control circuit can see this effect us a load perturbation but some times the normal operation of the dc-to-dc converter can be modified. This kind of operation will be called "abnormal". The consequences of these "abnormal operations" will be observed as an output voltage ripple higher than the expected. This output rippled is not related with the voltage ripple at the bulk capacitor, it is the result of the abnormal operation.

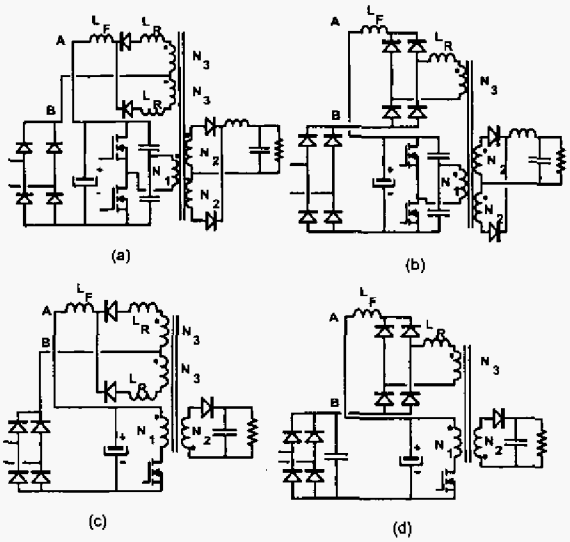

Fig. 2. Topologies with "abnormal operation"

The topologies shown in Fig. 2 were proposed in [3] and [4] and are in particular affected by the abnormal operation. These HINs can be used with symmetrically driven transformers (half-bridge, full-bridge and push-pull) and asymmetrically driven magnetics devices such as flyback, SEPIC and ZETA inductors. There are also other topologies with the same problem but can be obtained from these [7]. For instance, the circuit proposed in [6], a modified boost interleaved circuit, can be obtained from the topology shown in Fig. 2 (a) by removing the inductor called "L_F". Every topology complies with the IEC-61000-3-2 regulations, however, due to this abnormal work, and in order to obtain low output voltage ripple, the controller must be designed with special care.

In [8] a small signal model of these topologies is proposed. Nevertheless, the abnormal operation can only be observed in a

real model.

This paper deals with the abnormal operation, their effect and how to design the control system to solve the problem of output ripple.

2. NORMAL AND ABNORMAL OPERATION OF THE STUDIED TOPOLOGIES

As an example of abnormal operation, only the topology shown in Fig. 2(a) will be studied. Furthermore, the switching ripple will be neglected in the output current (I_{Lo}) and line current (I_g).

In order to understand the abnormal operation it is necessary to have a good knowledge of normal operation. Afterwards, small modifications due to the HIN will be introduced and finally the abnormal work will be shown.

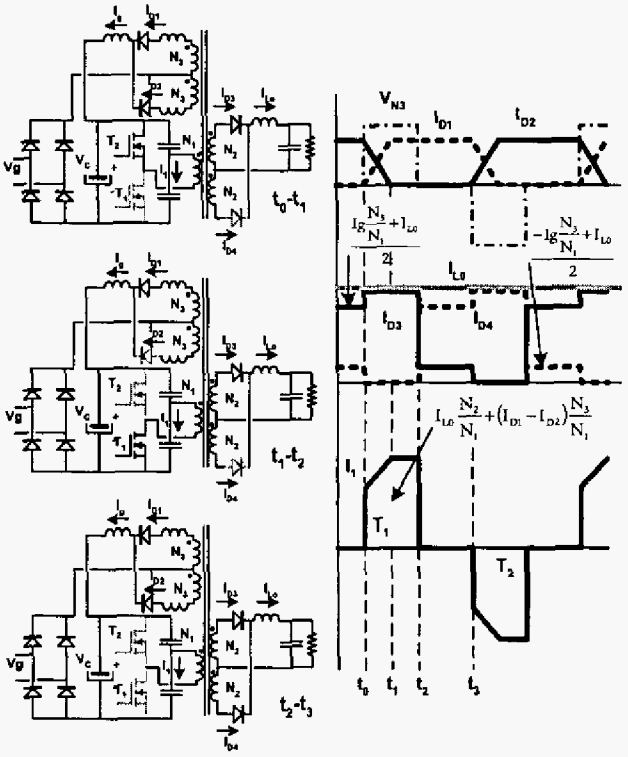

Fig. 3. Normal operation (half-bridge)

A. Normal operation of a half-bridge (Fig. 3)

Interval t_0-t_1

As can be seen from Fig. 3 (interval t_0-t_1) diodes D_1, D_2 and D_3 (in bold) are "on" until I_{D1} reaches I_g and D_2 turns off. This period can be calculated from (1)

$$t_1 - t_0 = I_g \cdot L_R \frac{N_1}{N_3}\frac{2}{V_C} \qquad (1)$$

Interval t_1-t_2

During this interval I_{D1} has the same value as I_g. This interval will finish when transistor T_1 is turned off.

Interval t_2-t_3

Immediately before transistor T_1 is turned off, the output current (I_{Lo}) will be shared out among D_3 and D_4. Therefore the voltage across winding N_3 is zero. Neglecting the magnetizing current, I_{D3} and I_{D4} can be calculated from equations (2) and (3).

$$I_1 N_1 + I_{D2} N_2 - I_{D1} N_3 + I_{D4} N_2 - I_{D3} N_3 = 0 \qquad (2)$$

$$I_{D3} + I_{D4} = I_{Lo} \qquad (3)$$

Without the HIN (and neglecting the magnetizing current) I_{D3} and I_{D4} would have a value equal to $I_{Lo}/2$. Due to the current flowing across windings N_3 and N_2, the expected current values are modified as can be seen from equations (4) and (5). These values are modified by I_{D2} which is equal to I_g during this interval. When current I_{D2} is increased to the level $I_{D2} > I_{Lo} N_2/N_3$, then diode D_3 turns off before the moment expected in normal operation. One of the abnormal operations has thus occured. The limit between the normal and abnormal operation is fixed by equation (6).

$$I_{D4} = \left(I_{D2}\frac{N_3}{N_2} + I_{Lo} \right)/2 \qquad (4)$$

$$I_{D3} = \left(-I_{D2}\frac{N_3}{N_2} + I_{Lo} \right)/2 \qquad (5)$$

$$I_g \geq \frac{N_2}{N_3} I_{Lo} \qquad (6)$$

B. Abnormal operation (I) of a half-bridge (Fig. 4)

The highest conduction angle (θ_c) to avoid this problem can be calculated from the preceding analysis of limits between normal and abnormal operation and by using the simplified models proposed by [3][4]. This maximum angle is 95° in the best case (Bulk capacitor voltage has the same value as peak line voltage, neglecting magnetizing currents and neglecting high frequency current ripple).

At instant t_2 during normal operation, currents flowing through diodes D_1 and D_2 (I_{D1} and I_{D2}) could share out among I_{D3} and I_{D4}. Now, as can be seen in Fig. 4 (interval t_2-t_3), the input current I_g is bigger than the limit value (6) so only one diode of the output rectifier is on. The extra current must find a new path, the inductor L_o has high impendace, them the only possible way is through the body diode of the upper-side transistor. During the interval (t_2-t_3) voltage is applied to winding N_1 and so this voltage is reflected in an increase of the duty cycle. This extra voltage applied to the load must be corrected by the control system.

In order to show the effects that the abnormal operation has caused on the output voltage, a half-bridge prototype has been built. Fig. 5 shows the input current (I_g) and the output voltage (V_{out}) measured for the same power (100W) but different line voltage ($190V_{rms}$ top and $230V_{rms}$ bottom) with constant duty

cycle. As can be seen on the top one, abnormal operation has not appeared and output voltage ripple waveform is the same as the bulk capacitor ripple. Nevertheless on the bottom one, the abnormal operation has appeared and the output voltage ripple has a different waveform. A similar result can be obtained by reducing the load.

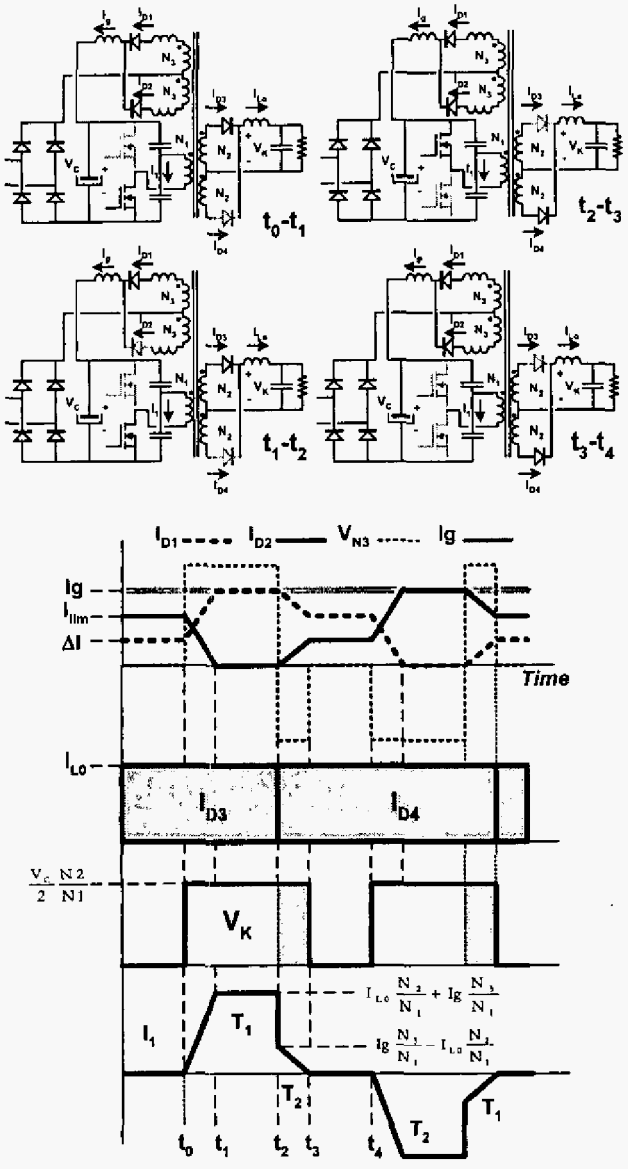

Fig. 4. Abnormal operation (I) for a half-bridge

When the difference between bulk capacitor's voltage and peak line voltage increases (due to load regulation [3][4]) the converter comes closer to the abnormal operation (I). Moreover, when the load is decreased, current ripple cannot be neglected and another abnormal operation appears.

C.Abnormal operation (II) of a half-bridge (Fig. 6)

As shows Fig. 6 output current ripple makes one of the output diodes turn off. So, during (t_0-t_1) an extra voltage is applied to the output. Since the HIN's diodes (D_1 and D_2) are both "on", the extra voltage (ΔV) can be calculated from equation (7).

$$\Delta V = Vout \frac{L_R}{L_R + 2\frac{L_0}{\left(N_2/N_1\right)^2}} \quad (7)$$

Both abnormal operation (I) and (II) can appear at the same time. Nevertheless, they have been shown separately for a simple explanation.

D. Abnormal operation of inductor coupled HIN.

There are also abnormal operations in inductor coupled HINs and although the magnetizing current in a flyback converter could be enough for continuous conduction mode (CCM), the HIN influence can turn off the output diode before the next switching interval. This "false" discontinuous conduction mode can be seen as an abnormal operation. The effect on the output voltage ripple is the same as for the previously explanation. But in this case, there is an additional problem: the flyback dynamics. Similar perturbations will be more difficult to mitigate in a flyback converter than in a half-bridge converter.

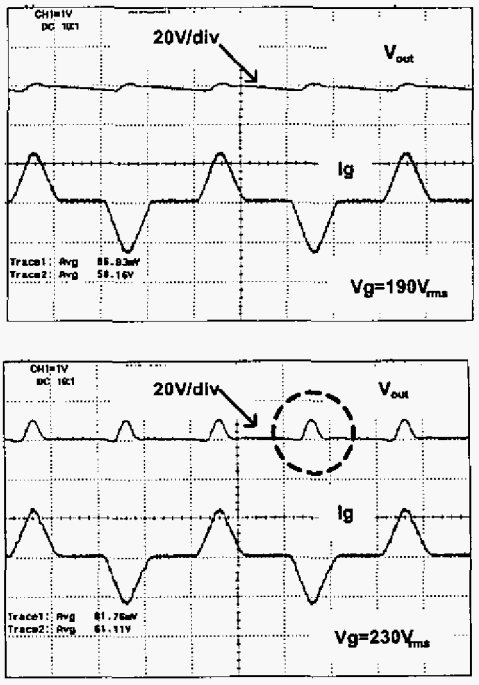

Fig. 5. Ig and Vout at full power (100W) with very slow voltage control for a half-bridge converter with different line voltages (Vg)

3. CONTROLLER DESIGN

In spite of having small signal ac models for these ac-to-dc converters [8], abnormal operations are not reflected in them. To obtain these models is a very difficult task so in this paper abnormal operation will be studied as load and input voltage

perturbations. In order to obtain the accurate control strategy, different control systems have been implemented on the same converter.

The topology shown in Fig. 2 (d) has been selected to test the different control strategies. The ac-to-dc converter has been designed to comply with IEC-61000-3-2 Class D. The output voltage is 54V, the input power 100W, the input line voltage is 190-230V_{rms} and the switching frequency 100 kHz.

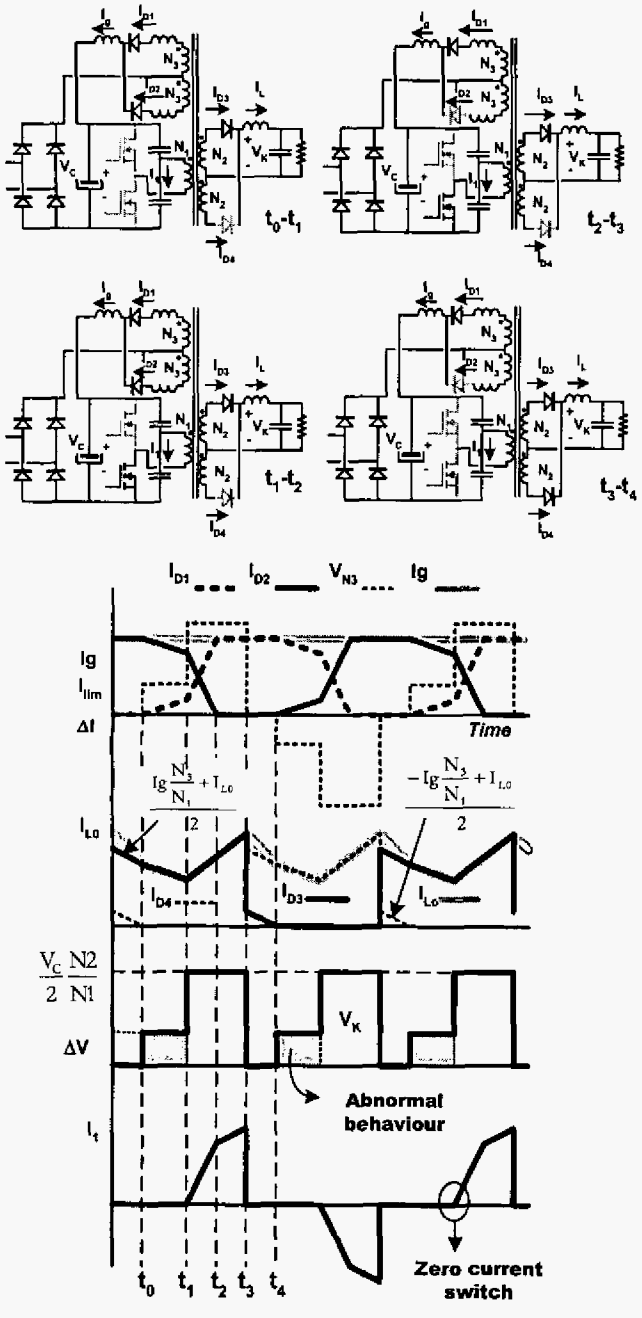

Fig. 6. Abnormal operation (II) of a half-bridge

Feedback loop for regulation of the output voltage.

The designed compensator has a crossover frequency of 5 kHz, large loop gain over the bandwidth of the feedback loop, and phase margin of 45°. This compensator should be enough for most normal designs, nevertheless, as can be seen from Fig. 7 (a), due to the HIN influence, the output voltage ripple is too big. As Fig. 7 (a.2) shows, this effect is more important for low loads where the voltage ripple is higher than 4% of the output voltage.

Averaged current programmed control

The results shown in Fig. 7 (b) have been obtained with an averaged current programmed control. The crossover frequency of the current loop and voltage loop were 15 kHz and 5 kHz, with a phase margin of 45°. As can be seen in Fig. 7 (b.2) even for the worst conditions the output voltage ripple is lower than 0.5% of the output voltage.

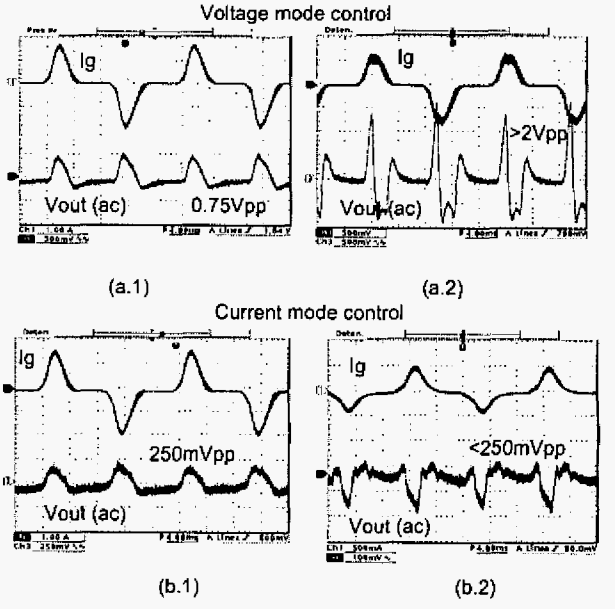

Fig. 7. Ig and Vout. (1)full load 100W (2) 25% load (25W)

4. CONCLUSIONS

The extra output voltage ripple presented in hasn't been study previously, probably because the converter test was made with full load and all the attention was focused on the input current and bulk capacitor voltage. Due to the study of abnormal operations it has been shown that these kind of S^2ICS's are not the best choice for low output voltage ripple applications with high conductions angles (Class D), nevertheless they are a good choice for low power Class A converters. In order to obtain an acceptable output ripple (for Class D converters) an averaged current programmed control must be used.

5. REFERENCES

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