Effect of the Output Impedance of Active Clamp Topology in Multiphase Converters

Esther de Jódar, José Villarejo, Juan Suardíaz, Fulgencio Soto
Departamento de Tecnología Electrónica
Universidad Politécnica de Cartagena
Cartagena, Spain
Email: esther.jodar@upct.es, jose.villarejo@upct.es, juan.suardiaz@upct.es, pencho.soto@upct.es

***Abstract*—Passive current sharing in multiphase converters, where resistive losses are not dominant, is a quite complex goal. In this paper an averaged model of an active clamp converter was obtained. It has been checked that these topologies present high output impedance. This property is used like a lossless passive equalization. Simulated results of the average model accuracy and current sharing are presented.**

I. INTRODUCTION

Increasing the frequency in switching converters is a trend to reduce size and weight. Nevertheless, higher frequency means higher switching losses. Different soft-switching solutions have been presented to minimize switching losses. One contribution is the active clamp topology [1], where Zero Voltage Switching (ZVS) is achieved by just adding an auxiliary switch, S_1, an LC resonant circuit and a clamp capacitor, C_1, as can be seen in Fig. 1 for a buck converter.

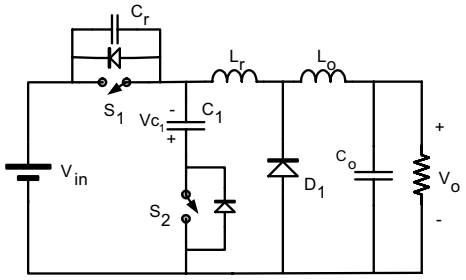

Fig. 1. Active clamp ZVS Buck converter.

The analysis of active clamp converters has been presented for different topologies [1-6]. A study of the effect of clamp capacitor on the stability of a flyback converter is studied in [7]. In [3] an averaged switching modeling is applied to predict the dynamic behavior of active clamp converters. In [8] a model for the active clamp family converters presented in [1] was submitted. In [8] it was proved that the active clamp converter works as impedance, but that model does not include clamp capacitor and soft-switching effects in the converter input.

Here, a complete model is presented, following the method shown in [3]. In this work the clamp capacitor is comprised in the model. As well as that it has been taken into account the effect of the dead time, needed for the existence of soft switching, [2], and the errors introduced in the model by the time interval between the turning-on of S_1 and the turning-off of S_2,. It is also proposed an application of the active clamp buck converter for multiphase converters design, taking advantage of the output impedance, working as lossless equalizing resistor. So no current control loop for each phase is needed.

To deduce the small-signal behavior of the converter, an averaged modeling method will be used in Section II. Converter's transfer function and output impedance will be obtained. Principle of operation will be shown to understand how the converter behaves. An example of current sharing in multiphase converters is presented in Section III.

II. AVERAGED SWITCH MODELING

A. Principle of Operation

To simplify the analysis, the output filter inductance, L_o, is large enough to be considered as a current source, clamp capacitor, C_1, is considered as a constant voltage source, Vc_1. The circuit works in CCM and both switches, S1 and S2, are turned on and off in a complementary way. The converter ideal waveforms can be found in Fig. 2.

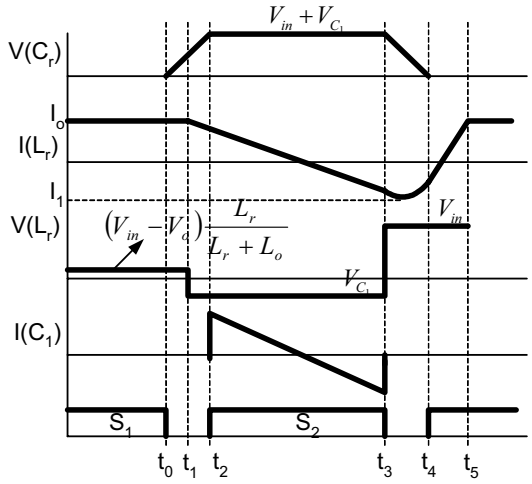

Fig. 2. Converter ideal waveforms

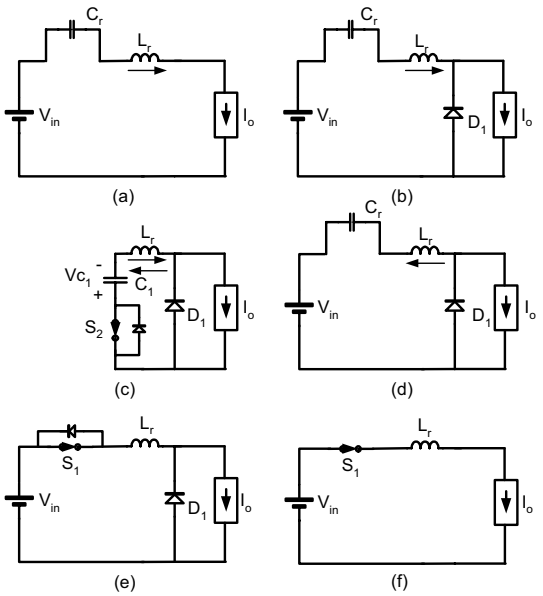

Fig. 3. Stages in a switching period. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6

A switching period can be divided into 6 stages, Fig. 3:

Stage 1 (t_0-t_1). Before t_0, S_1 is on and S_2 is off. At t_0 S_1 is turned off and C_r is lineally charged to V_{in}.

Stage 2 (t_1-t_2). When C_r reaches V_{in}, the free-wheeling diode, D_1, is forward biased. The current through L_r and C_r evolves in a resonant way and the voltage in C_r rises to $V_{in}+V_c$.

Stage 3 (t_2-t_3). S_2 turns on with no losses. Current through L_r ramps down. S_2 is turned off at t_3.

Stage 4 (t_3-t_4). The voltage across C_r falls to zero, due to resonance with L_r.

Stage 5 (t_4-t_5). S_1 is turned on with zero voltage and without losses because the voltage at C_r is null. The current through L_r changes the polarity and ramps up until it reaches I_o.

Stage 6. The diode, D_1 is reversed biased. At the end of this stage S_1 is turned off, being the end of a switching period.

A more detailed explanation of circuit operation can be found in [1].

B. Average Model.

In order to obtain the model, currents and voltages are averaged in a switching period. Switches will be replaced by dependent current and voltages sources, in terms of duty cycle and other converter parameters. To simplify, resonant transitions are ignored.

Current through Lr, Fig. 2, during the interval from t_3 to t_5 will be

$$\frac{V_{in}}{L_r}\cdot t_{3-5} = I_{L_o} - I_1 \tag{1}$$

In steady-state $I_1 = I_{Lo}$. If I_1 is not included the dynamic effect of C_1 is neglected.

Voltage through clamp capacitor can be considered constant in a switching cycle so

$$\frac{V_{C_1}}{L_r}\cdot(1-d)\cdot T_s = I_{L_o} - I_1 \tag{2}$$

From (1) and (2) (3) can be obtained

$$\frac{t_{3-5}}{T_s} = \frac{V_{C_1}\cdot(1-d)}{V_{in}} \tag{3}$$

So, the average current through the output capacitor is

$$\left\langle i_{C_o}\right\rangle = C_o\frac{dv_o}{dt} = \left\langle i_{L_o}\right\rangle - \frac{\left\langle v_o\right\rangle}{R} \tag{4}$$

As the resonant inductance, L_r, is negligible related to the output filter inductance, L_o, the voltage drop through L_r when S_1 is off will be neglected

$$\left\langle v_{L_o}\right\rangle = -v_o\frac{t_{3-5}}{T_s} + (v_{in}-v_o)\frac{dT_s - t_{3-5}}{T_s} - v_o(1-d) \tag{5}$$

Replacing (3)

$$\left\langle v_{L_o}\right\rangle = L_o\frac{di_{L_o}}{dt} = v_{in}d - v_{C_1}(1-d) - v_o \tag{6}$$

Average clamp capacitor current, Fig. 2, is

$$C_1\frac{dv_{C_1}}{dt} = (I_{L_o}+I_1)\frac{(1-d)}{2} \tag{7}$$

And from (2) it can be seen

$$C_1\frac{dv_{C_1}}{dt} = I_{L_o}(1-d) - \frac{v_{C_1}}{2L_r f_s}(1-d)^2 \tag{8}$$

For an easy analysis the input current has been divided in several stages, in that way, there is a subinterval from t_3 to t_5 where

$$\left\langle i_{in}\right\rangle_{t_{3-5}} = \frac{1}{T_s}\int_o^{t_{3-5}}\left(I_1 + \frac{I_o - I_1}{t_{3-5}}t\right)dt \tag{9}$$

With (3) and (1) it takes to

$$\left\langle i_{in}\right\rangle_{t_{3-5}} = I_{L_o}\frac{V_{C_1}(1-d)}{V_{in}} - \frac{V_{C_1}^2}{V_{in}}\frac{1}{R_{eq}} \tag{10}$$

where R_{eq} is

$$R_{eq} = \frac{2L_r f_s}{(1-d)^2} \tag{11}$$

So, the average input current is

$$\langle i_{in} \rangle_{T_s} = I_o d - \frac{V_{C_1}^2}{V_{in}} \frac{1}{R_{eq}} \tag{12}$$

From (4), (6), (8) and (12) the averaged equivalent circuit is shown at Fig. 4.

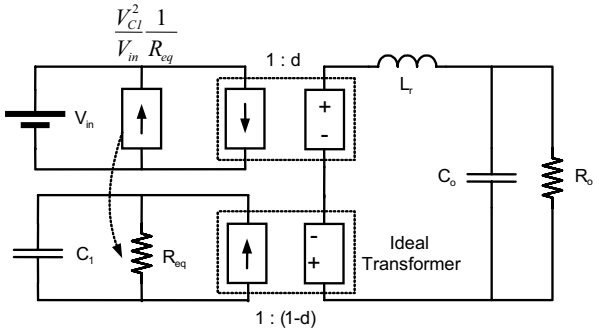

Fig. 4. Average model.

C. *Small Signal Model*

The averaged model obtained at previous section is clearly non lineal. After linearization of (4), (6) and (8), defining the steady-state equilibrium as (D, V_{in}, V_o, V_{C1}, I_{Lo}), the system state-space representation, where *u* is the vector of inputs, *y* is the system output and *x* is the status variables vector, is

$$\dot{x} = Ax + Bu \tag{13}$$

$$y = Cx + Du \tag{14}$$

Where $x = [i_{Lo}\ v_{C1}\ v_o]^T$, $u = [v_{in}\ d]^T$, $y = v_o$, where

C = [0 0 1], D = [0] and

$$A = \begin{bmatrix} 0 & \frac{-(1-D)}{L_o} & -\frac{1}{L_o} \\ \frac{1-D}{C_1} & -\frac{1}{R_{eq}C_1} & 0 \\ \frac{1}{C_o} & 0 & \frac{-1}{RC_o} \end{bmatrix} \quad B = \begin{bmatrix} \frac{D}{L_o} & \frac{V_{in}+V_{C_1}}{L_0} \\ 0 & \frac{V_{C_1}}{L_r f_s C_1}(1-D) - \frac{I_{L_o}}{C_1} \\ 0 & 0 \end{bmatrix}$$

The small signal equivalent circuit is represented in Fig. 5.

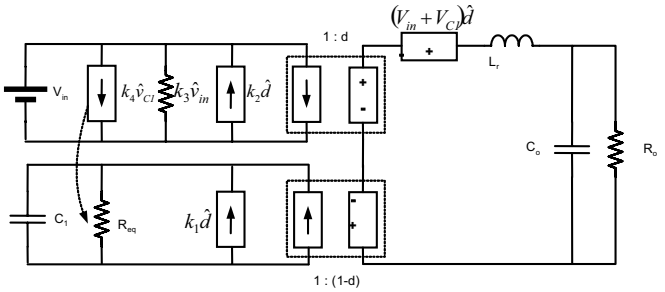

Fig. 5. Small signal model.

Now, the converter transfer functions, G_{vg} and G_{vd}, can be derived from the lineal system

$$[G_{vg}(s)\ G_{vd}(s)] = C(sI-A)^{-1}B \tag{15}$$

Constants k_1, k_2… from the small signal model in Fig. 5 can be found in Table I

TABLE I
CONVERTER SMALL SIGANL MODEL

Parameter	Value
k_1	$\frac{V_{C_1}}{L_r f_s}(1-D) - I_{L_o}$
k_2	$I_{L_o} + \frac{2V_{C_1}^2}{V_{in}} \frac{1}{2L_r f_s}(1-D)$
k_3	$-\frac{V_{C_1}^2}{V_{in}} \frac{1}{R_e}$
k_4	$2\frac{V_{C_1}}{V_{in}} \frac{1}{R_e}$

The Bode diagram at Fig. 6 represents the control-to-output transfer function, G_{vd}, for different clamp capacitors, C_1. It can be checked that the output changes as a result of variations of clamp capacitor, so, its inclusion in the model is justified.

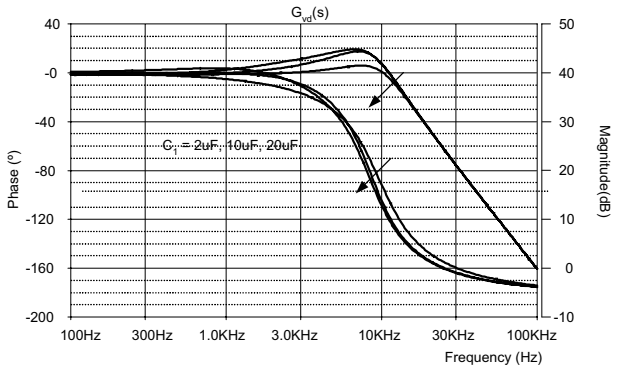

Fig.6. G_{vd} Bode diagram. Magnitude and phase for different clamp capacitors

D. Averaged model validation

A simulation has been performed to estimate how accurately the model matches the converter. Converter parameters can be found at Table II.

TABLE II
CONVERTER OPERATING VALUES

Parameter	Value	Parameter	Value
V_{in}	120 V	C_o	4 µF
V_o	48 V	L_o	86.4 µH
D	0.5	C_r	2 nF
f_s	100 kHz	L_r	6 µH
P	480 W	C_1	2 µF
R	4.8 Ω		

The converter dynamic response to a duty cycle step is represented in Fig. 7 and 8, where it can be noted that currents and voltages in the average model are in good agreement with current and voltages in the simulated switched converter.

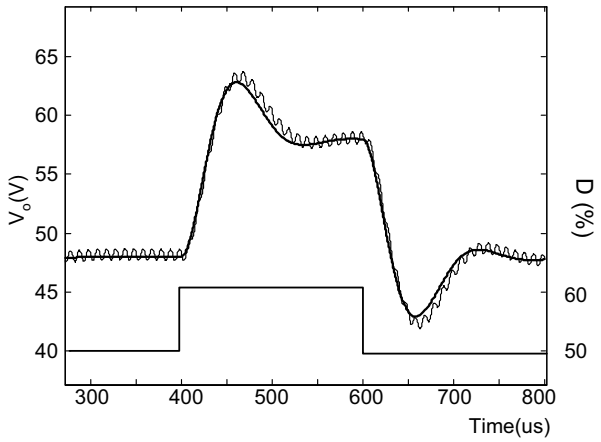

Fig. 7. Converter output voltage and average model voltage

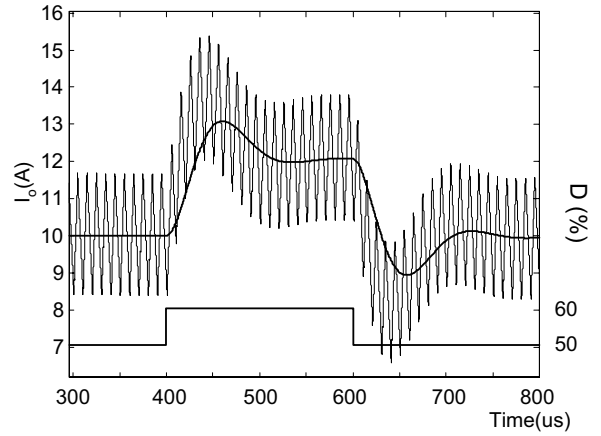

Fig. 8. Converter output current and average model current

For the existence of soft commutation it is necessary to have a dead time between the turning-on of S_1 and the turning-off of S_2. The proposed averaged model is in accordance with the switched converter when the "time delay" shown in Fig. 9 is close to zero. The effect introduced by the "time delay" is to increase the "effective" duty cycle. So, it can be noticed for large duty cycles and high frequencies.

In Fig. 10 the difference between the converter output voltage and the averaged voltage can be seen, when the dead time is excessive.

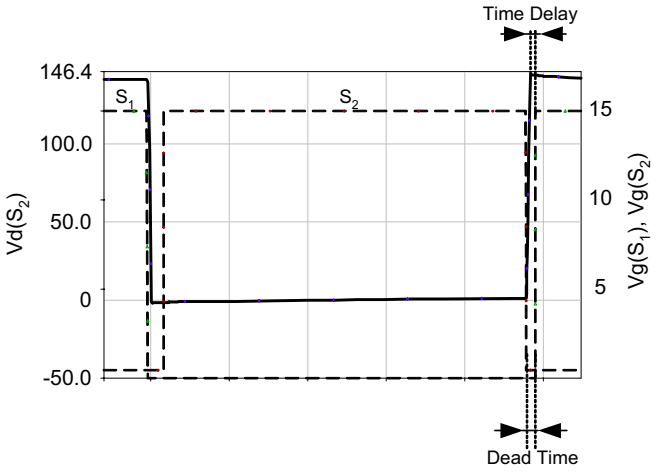

Fig. 9. Dead time between S_1 and S_2.

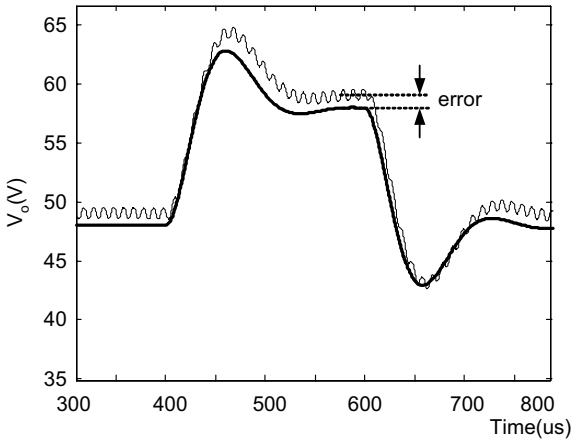

Fig. 10. Error between the converter and averaged model

E. Output impedance

The output impedance, $Z_o(s)$, can be obtained if in the previous state-space representation of the system, (13) and (14), the inputs are defined now as $u = [v_{in}\ d\ i_o]^T$ and the current through the output filter capacitor, (4), is replaced by

$$i_{C_o} = C_o \frac{dv_o}{dt} = i_{L_o} - i_o, \tag{16}$$

The output impedance is represented in the Bode diagram, shown in Fig. 11. The DC output impedance can be noticed

$$Z_{o(DC)} = 2L_r f_s = R_{eq}(1-D)^2 \tag{17}$$

which is the defined equivalent resistor, R_{eq}, seen from the secondary side.

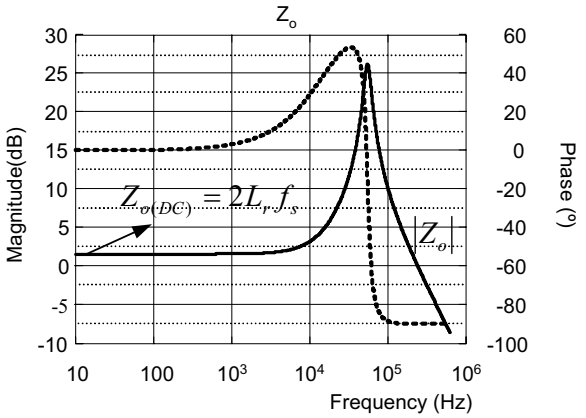

Fig. 11. Output impedance.

In another way a DC output characteristic is

$$\frac{V_o}{V_{in\,(DC)}} = \frac{RD}{R + 2L_r f_s}, \tag{18}$$

So it can be derived as a connection between the output voltage and input voltage

$$V_{o(DC)} = V_{in} D - 2L_r f_s I_o, \tag{19}$$

that connects both voltages, V_o and V_{in}, with the converter output impedance.

III. MULTIPHASE ACTIVE CLAMP BUCK CONVERTER

Passive current sharing can be used successfully with synchronous converters with digital PWM, where there is a perfect matching of the duty cycles of the PWM signals among the different phases, [9]. With these conditions, the transistors, conductors and inductors internal resistor will be large enough to equalize the currents.

In addition, temperature will have an equalizing effect. If there is a phase with a higher current it will have a higher temperature and its resistance will be increased, which means to a better current sharing. But in topologies with higher output voltages, where free wheeling diodes are used, the temperature effect is completely different.

If there is a difference among the diodes forward voltages in a multiphase converter that difference will be increased. Higher current will flow through the phase that has a diode with smaller forward voltage and, with an increasing temperature, the forward voltage will be decreased.

To prove the effect in a multiphase active clamp converter with diodes, a simulation was carried out to check the current deviation from the nominal value. If the forward voltage of one diode has a deviation of 40% from the others and considering the output filter inductors, L_o, as non ideal, with an internal resistor with a value of 0.05Ω. In Fig. 12 the current sharing in a multiphase buck converter without active clamp can be seen.

In the multiphase Buck converter without active clamp the current deviation due to a smaller forward voltage is

$$(\Delta I)_{diode} = \frac{n-1}{n} \frac{\Delta V_{diode}}{R_{eq}} (1-D) \tag{20}$$

and, as Fig. 12 shows, here, with n = 3 phases, a voltage deviation of 40% in one phase diode and D = 0.5, results in a current deviation of 2 Amps in that phase.

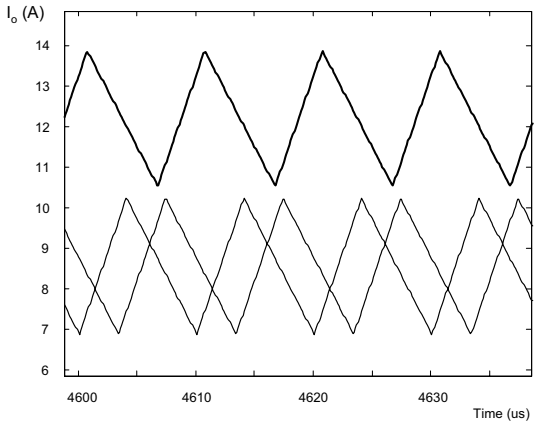

Fig. 12. Current sharing in a 3 phase buck converter without active clamp for different diode drop voltage

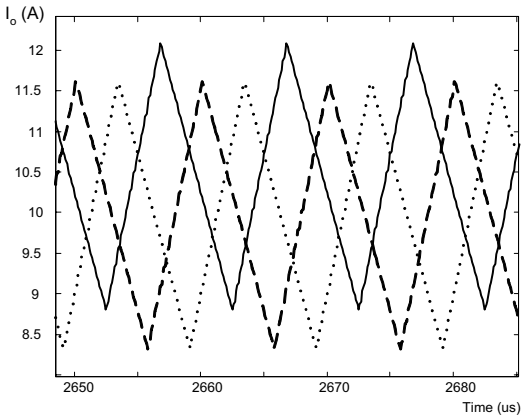

Fig. 13. Current sharing in a 3 phase buck converter with active clamp for different diode drop voltage

For a multiphase active clamp buck converter, with the same deviation in the components, it can be proved that there is a better current sharing among phases than in a converter without active clamp, Fig. 13. From (19) it can be seen that the active clamp increases the output impedance. In this way, the converter acts as a voltage source with high output impedance. As the converter output impedance, Z_o, is higher than the other impedances in the circuit, it will act as an equalizing resistor without losses and it will achieve the current sharing.

A design criterion for the multiphase converter can be to set a maximum difference among currents when there is a mismatch in the duty cycle. A three phase converter was designed that must have a deviation of 1 A from the nominal output current if there is a maximum deviation of 2% from the nominal duty cycle.

The converter output characteristic, (19), is represented in Fig. 14. The nominal duty cycle is 0.5 and two phases present a 2% deviation from the nominal. Under these conditions, the phase with nominal duty cycle must have an output current of 10 Amps and, because of duty cycle mismatching, phases with a 2% deviation in duty cycle must have 1 Amps under or above the nominal output current.

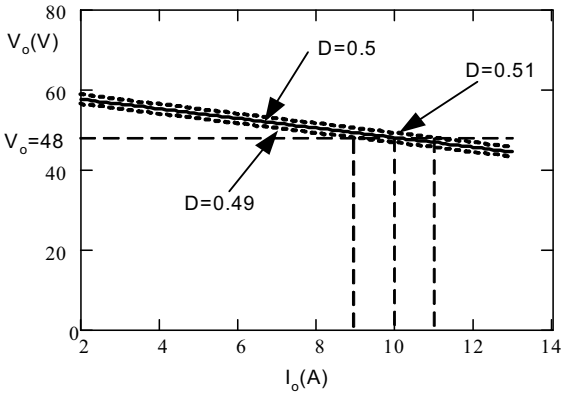

Fig. 14. DC output characteristic and current equalization.

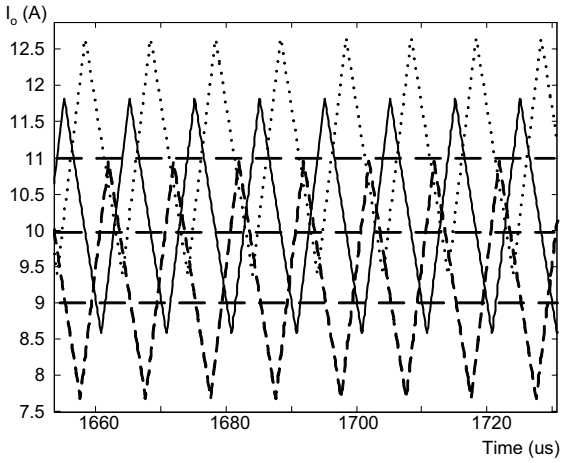

Fig. 15. Current sharing in a 3 phase buck converter with active clamp.

Current sharing in a three phase active clamp buck converter is shown in Fig. 15. The output current has been shown for each phase and average output current. Therefore, it can be noticed that the equalized currents and the converter behavior is in accordance with the design method.

IV. CONCLUSION

Active clamp converter models presented until now have been revised and an improved model, including clamp capacitor, of the one presented in [8] has been proposed. The converter output impedance and a possible application to multiphase converters have both been studied.

A prototype is being implemented to test the results obtained in simulations.

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