New implementations of Single-Stage Power-Factor-Correctors with Voltage-Doubler Line Rectifier

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***Abstract*-This paper deals with a new implementation of a Voltage-Doubler Single-Stage Power Factor Corrector (VD-S²PFC). This new VD-S²PFC provides a reduction (by half) of the total voltage drop due to diodes conducting at the same time from the line input to the energy-storage capacitors. Moreover, the size of the additional inductors used to shape the line current is dramatically reduced due to the fact that these inductors form part of an additional output of the main dc-to-dc converter, which is based on a full-wave rectifier and, therefore, these inductors are operating at twice the converter switching frequency and with a higher duty cycle than in the case of being based on a half-wave rectifier, as in some previous cases. The experimental results show that both inductors can be built into two E20 cores for a 100 W, 62 V_{dc} prototype. The voltage across the series connection of both energy-storage capacitors is lower than 500V and the total efficiency of this prototype is 92-90%.**

I. INTRODUCTION

Many Single-Stage Power Factor Correctors (S²PFCs) [1-8] (see Fig.1) have been recently proposed to achieve both the standard dynamic behaviour of conventional dc-to-dc converters and the desired compliance with the regulations (especially with the IEC-1000-3-2). When the ac input voltage changes in a moderate range (for example in either the American or the European range), S²PFCs are very attractive, because they combine fast output voltage regulation and moderate input current harmonic content. It should be noted that both characteristics are achieved in S²PFCs maintaining the cost and the complexity of the circuit relatively low. However, if standard S²PFCs are designed to operate in universal-line applications (85-265 Vac), they become less attractive due to variations of the voltage across the energy-storage capacitor with load and, especially, with input voltage. These variations cause two negative effects:

- A detrimental effect on the conversion efficiency [9], because the voltage across the energy-storage capacitor is also the input voltage of the dc-to-dc converter part of the S²PFC.
- A relatively large size of the energy-storage capacitor [9] because its capacitance must be high enough to meet the hold-up time requirements at low voltage (110Vac) and its voltage rating must be around 450Vdc.

These drawbacks can be partially overcome by modifying some S²PFC topologies to use a line rectifier that can operate as a conventional line rectifier in the European range and as a voltage-doubler line rectifier in the American range. This option was presented in [10, 11] applied to the topologies studied in [3-5]. Other very attractive implementations of Voltage-Doubler Single-Stage Power factor Correctors (VD-S²PFCs) have been presented in [12] (see Fig. 2a and 2b). In this paper, a new implementation of VD-S²PFC is going to be presented (see Fig. 2c). This new VD-S²PFC has the following advantages over the previous ones:

- Only two diodes (instead of four in [10-12]) are

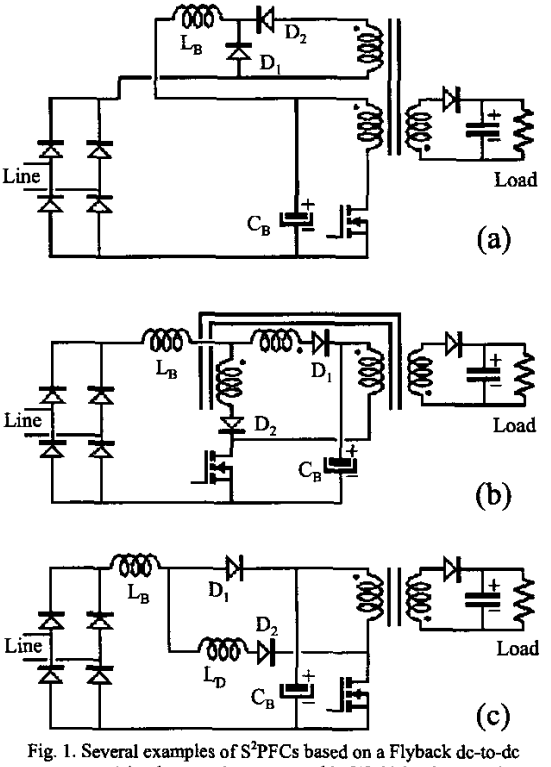

Fig. 1. Several examples of S²PFCs based on a Flyback dc-to-dc converter: a) implementation presented in [1]; b) implementation presented in [3,4]; c) implementation presented in [5,6].

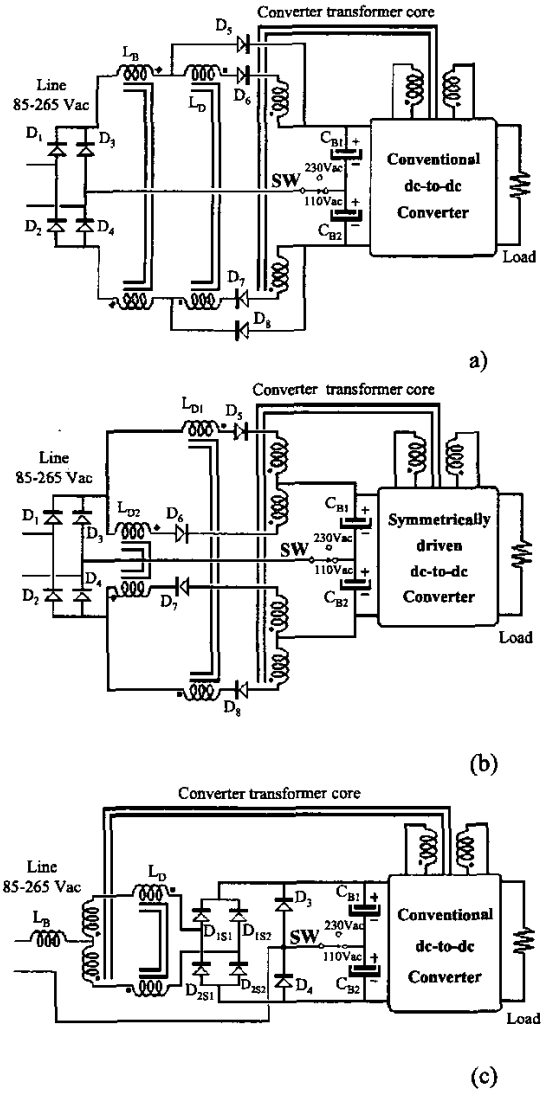

Fig. 2. Several VD-S^{2}PFCs: a) implementation presented in [11]; b) implementation presented in [12]; c) implementation presented in this paper.

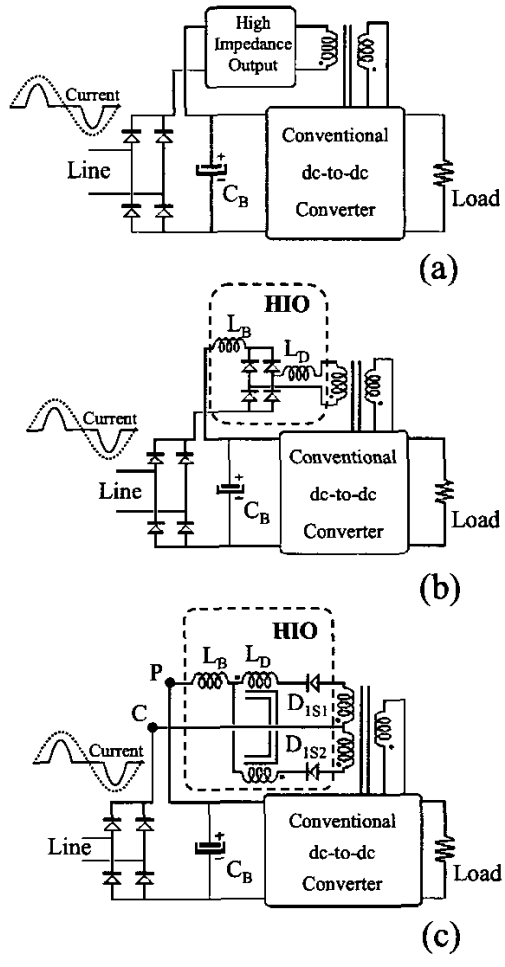

Fig. 3. a) General scheme for many S^{2}PFCs; b) implementation presented in [7, 8] for the European range; c) implementation presented in [7, 8] for the American range.

connected in series between the line input and the energy-storage capacitors. In the previous VD-S^{2}PFCs, two diodes are conducting together in the American range (SW closed) and four are conducting together in the European range (SW open). These numbers are divided by two in the proposed topology.

- All the additional inductors added to shape the line current operate at twice the switching frequency. This occurs not only with symmetrically-driven topologies (such as half-bridge, full-bridge and push-pull) but also with some asymmetrically-driven topologies (such as flyback, SEPIC and Cuk). As a result of the higher switching frequency operation, the total size of the additional inductors is very small, even if the boost inductor L_B has been designed to operate in Continuous Conduction Mode (CCM).

II. Modifying Single-Stage Power-Factor-Correctors to Improve Their Efficiency at Low Line Voltage by Integrating High-Frequency and Line-Rectifier Diodes

Several types of S^{2}PFCs are based on the connection of an additional "High-Impedance Output" (HIO) between the input rectifier and the energy-storage bulk capacitor C_B (see Fig. 3a). This HIO can be implemented in several different ways. Two attractive implementations are shown in Fig. 3b-c, [7-8]. The total size of the additional inductors L_B and L_D is slightly lower in the first implementation (Fig. 3b), but two high-frequency diodes and two line-rectifier diodes are connected in series between the input line and the energy-storage bulk capacitor C_B. On the other hand, the two high-frequency diodes are reduced to only one in the second implementation (Fig. 3c). Therefore, the former is more attractive for the European range of input voltage (where the voltage drop across the diodes is less

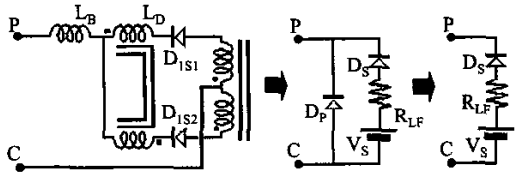

Fig. 4. Process to obtain the equivalent circuit of the HIOs shown in Fig. 3b-c.

significant), whereas the latter is more attractive for the American and Japanese range.

However, the number of diodes conducting simultaneously can be reduced again by integrating the HIO high-frequency diodes and the line-rectifier low-frequency diodes. Figure 4 shows the equivalent circuit for the HIOs shown in Fig. 3b-c. This equivalent circuit consist of a voltage source V_S, a loss-free resistor R_{LF} [6-8] and two diodes, a series diode D_S and a parallel diode D_P. The function of D_S in this equivalent circuit is to represent the fact that the current can only flow from the positive terminal P to the common terminal C (as in any additional converter output with diodes), whereas the function of D_P is to represent the fact that the output voltage cannot reverse (the same as in any additional converter output with diodes). A proper design of the HIO according to [6-8] results in D_P always being reverse biased and, therefore, it cannot be used for integration purposes. Therefore, the final equivalent circuit to start the integration process will be the one shown in Fig. 4c. Figure 5a shows the general scheme given in Fig. 3a with this equivalent circuit. As can be easily deduced from this figure, there is current passing through R_{LF} and V_S either when the couple of diodes D_{R1}-D_{R4} or the couple of diodes D_{R3}-D_{R2} are conducting. This means that the integration process of D_S as one of the diodes of the couples D_{R1}-D_{R4} or D_{R3}-D_{R2} will imply the duplication of R_{LF} and V_S.

Figure 5b shows one of the possible integrated options. Two sets of elements R_{LF}, V_S and D_S have been used to eliminate the rectifier diodes D_{R1} and D_{R2}. Now, only two

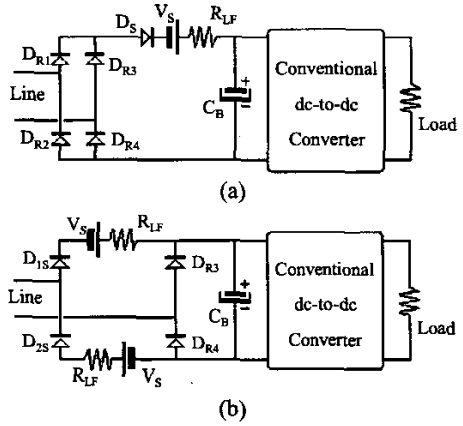

Fig. 5. a) Equivalent circuit for converters with the HIOs shown in Fig. 3b-c. b) Equivalent circuit after integrating high-frequency and line-rectifier diodes.

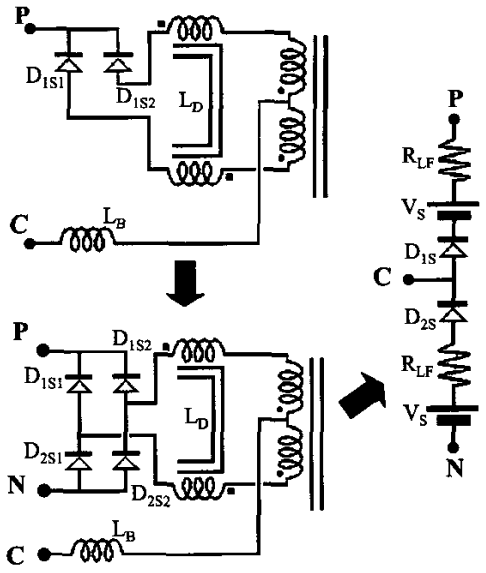

Fig. 6. Process to obtain two sets of elements D_S, V_S and R_{LF} from a HIO.

diodes (the couple D_{1S}-D_{R4} or the couple D_{R3}-D_{2S}) are conducting at the same time, whereas three diodes (either D_{R1}-D_S-D_{R4} or D_{R3}-D_S-D_{R4}) were conducting at the same time with the previous circuit (Fig. 5a).

The implementation of the new rectifier leg with two sets of elements R_{LF}, V_S and D_S can be obtained by duplicating all the elements of a HIO. However, a more attractive option is to avoid the duplication of the HIO magnetic elements. Figure 6 shows the steps to do this:

- The first step is to move L_B from the positive terminal P to the common terminal C.
- The second step is to obtain not only a positive output, but also a negative one. Diodes D_{1S1} and D_{1S2} in Fig. 6a-b are in charge of generating the positive output, whereas diodes D_{2S1} and D_{2S2} are in charge of generating the negative one. When the current flows from terminal P to terminal C, either D_{1S1} or D_{1S2} (depending on the voltage across the transformer) are conducting, whereas neither D_{2S1} and D_{2S2} are conducting. The situation is just the opposite when the current flows from terminal C to terminal N (either D_{2S1} or D_{2S2} are conducting, whereas both D_{1S1} and D_{1S2} are not conducting). Therefore, the elements of the HIO (that is, inductors L_B and L_D and the additional transformer winding) are alternatively connected between terminals P and C (when the current flows from P to C) and between terminals N and C (when the current flows from C to N). Therefore, the equivalent elements R_{LF} and V_S alternatively can be seen to be connected between either terminals P and C or terminals N and C. This is just the effect desired. The equivalent circuit is the one shown in Fig. 6c.
- The third step in the integration process is to substitute the two sets of equivalent elements R_{LF}, V_S

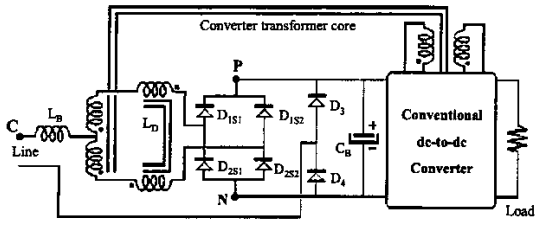

Fig. 7. New version of the converter shown in Fig. 3c after integrating high-frequency and line-rectifier diodes.

and D_S in Fig. 5b for the real elements shown in Fig. 6b. The final implementation is given in Fig. 7. From this figure, it can be deduced that only one high-frequency diode and one line-rectifier diode are conducting at the same time. Thus, in the positive half-cycle of the line voltage, either D_{1S1} or D_{1S2} (depending on the voltage across the converter transformer) and D_4 are conducting. The same occurs in the negative half-cycle, but for either D_{2S1} or D_{2S2} and D_3.

The procedure to design the turns ratio of the additional transformer winding and inductors L_D and L_B is exactly the same as shown in [6-8]. However, the high-frequency diodes D_{1S1}, D_{1S2}, D_{2S1} and D_{2S2} must be rated to withstand the input voltage of the dc-to-dc converter, which is in practice a higher voltage than the voltage withstood by the high-frequency diodes D_{1S1} and D_{1S2} in Fig. 3b.

Having only the voltage drop corresponding to two diodes instead of three improves the converter efficiency. This improvement is more significant for converters designed to operate only from the American and Japanese lines than for converters designed to operate only from the European line. However, this improvement is not the main advantage of the converter shown in Fig. 7, but rather its adaptability to operate with a line voltage-doubler at the input.

III. A New Topology of Voltage-Doubler Single-Stage Power-Factor-Corrector

The circuit shown in Fig. 7 can be easily adapted to be used with a voltage-doubler (see Fig. 2c). The operation of the line rectifier is as follows:

- When the range switch SW is in the "110Vac" position, D_3 and D_4 never conduct because they are reverse biased by C_{B1} and C_{B2}. The bulk capacitor C_{B1} is charged during the positive interval of the line voltage through one of the diodes D_{1s} (either D_{1s1} or D_{1s2}), the additional inductors and the additional transformer winding. The same occurs for C_{B2} during the negative interval, but the diode involved in the process is either D_{2s1} or D_{2s2}. Due to circuit symmetry, both capacitors are identically charged. The voltage across the input of the dc-to-dc converter will be twice as large as the voltage across one bulk capacitor. Finally, it should be noted that only one diode voltage drop is placed between the line input and the energy-storage bulk capacitors at the same time.
- When SW is in the "230Vac" position, both bulk capacitors are charged together. The diodes involved in the conduction process are D_4 (during the positive half-cycle) and D_3 (during the negative one). In this case, two diodes (one high-frequency diode and one line-rectifier diode) are conducting at the same time.

The design procedure of inductors L_B and L_D and of the turns ratio of the additional winding is the same as the one presented in references [6-8]. However, the effect of the voltage doubler must be taken into account only to calculate those dc-to-dc converter parameters that must be calculated at minimum line voltage (e.g. maximum converter duty cycle, transformer turns ratio, etc) and to compute the evolution of the voltage across the input port of the dc-to-dc converter properly.

The design procedure presented in references [6-8] assumes that the inductance of L_B is several times (3-5) as high as the inductance of L_D. However, the inductance of L_B can be chosen lower than the values proposed in these references, according to the design procedure shown in [13]. Thus, choosing L_B approximately equal to $L_D/4$, a good trade-off between input current ripple and inductor size can be established. Moreover, it should be noted that both inductors form part of an additional output (the HIO) based on a full-wave rectifier, which means that the magnetic elements used to modulate its output voltage according to the line current (that is, L_D) and the filter inductor L_B will be lower than in the case of using a half-wave rectifier [10, 11]. In other words, the HIO is operating at twice the converter switching frequency and the HIO duty cycle is higher than in the case of previous HIO based on a half-wave rectifier. Due to these facts, the final size of these inductors is quite small (for example, two E20 cores can be used to implement them for a 100W converter).

IV. Experimental Results

A prototype of the converter proposed (see Fig. 8) has been built and tested. As this figure shows, the "Conventional dc-to-dc Converter" in Fig. 2c is a half-bridge converter in this prototype. The input line voltage can be either the American range (85-130 V) or the European one (190-265 V), depending on the position of the mechanical range switch SW. The output is 62 V. Figure 9 shows the evolution of voltage across the energy-storage capacitors (that is, at the input port of the dc-to-dc converter) in this prototype. As Fig. 9 shows, this voltage is always lower than 500 Vdc and, therefore, two 180 μF/300 V capacitors can be used. Converter efficiency and the main waveforms at 110 Vac and 230 Vac are shown in Fig. 10 and 11, respectively. Finally, harmonic content complies with the IEC 1000-3-2 regulations (Class D) at 230 Vac and with the modified version of these regulations at 110 Vac, as Fig. 12 shows.

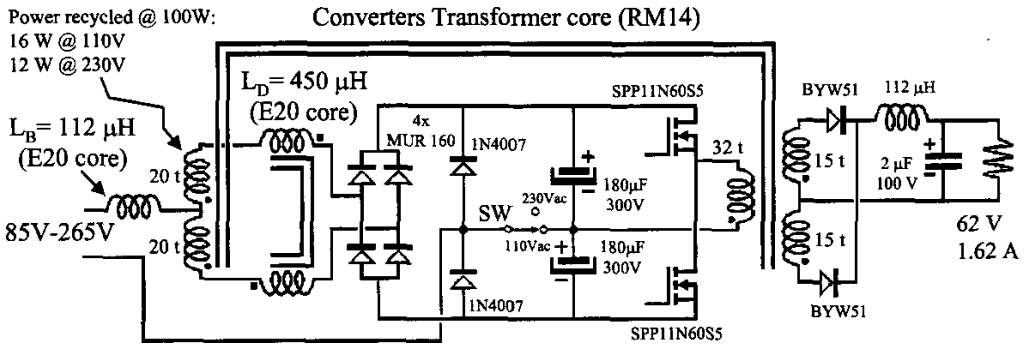

Fig. 8. Converter prototype.

V. CONCLUSIONS

A new implementation of a Voltage-Doubler Single-Stage Power Factor Corrector (VD-S^2PFC) has been presented in this digest. This new VD-S^2PFC allows a reduction (by half) of the total voltage drop due to diodes conducting at the same time from the line input to the energy-storage capacitors. Moreover, the size of the additional inductors used to shape the line current is reduced due to the fact that these inductors form part of an additional converter output (which has been designed as HIO), which operates at twice the converter switching frequency, and also to the fact that the HIO duty cycle is higher than in the case of previous HIOs based on a half-wave rectifier. Experimental results show that both inductors can be reasonably built into two E20 cores for a 100 W, 62 V_{dc} prototype. Finally, the voltage across the series connection of both energy-storage capacitors is lower than 500V and the total efficiency of this prototype is 92-90%.

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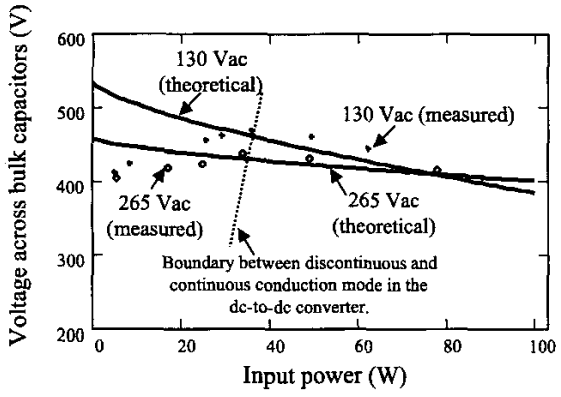

Fig. 9. Theoretical (solid lines) and experimental (dots) values of the voltage across the energy-storage bulk capacitor. Theoretical values have been obtained assuming CCM operation for any input power.

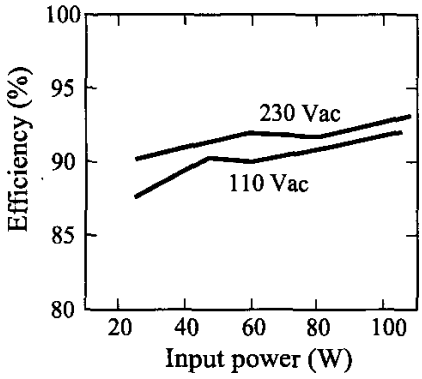

Fig. 10. Prototype efficiency

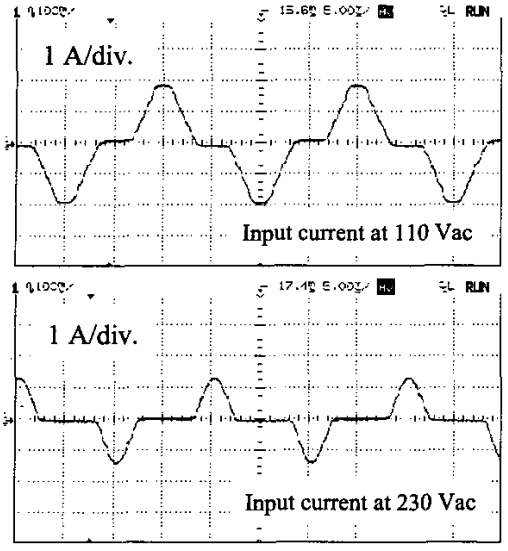

Fig. 11. Measured input current at full load.

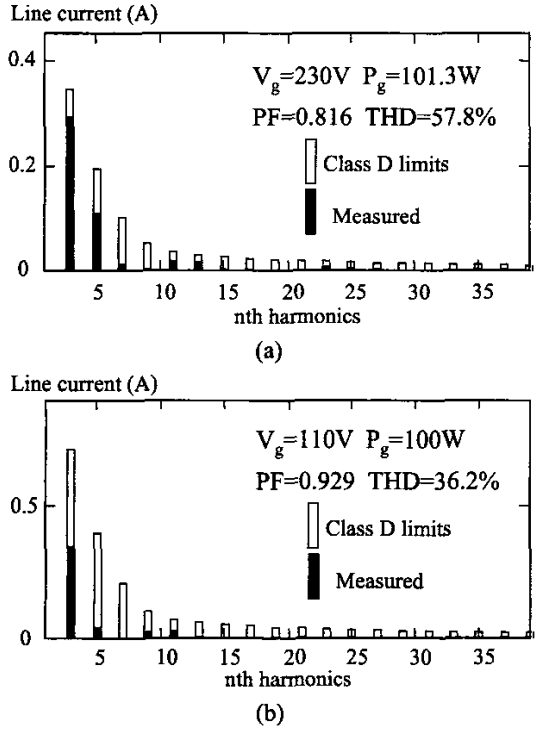

Fig. 12. a) Harmonic content at 230 Vac compared to the limits specified in the IEC 1000-3-2 regulation in Class D (Class A is less restrictive). b) Harmonic content at 110 Vac compared to the limits specified in the IEC 1000-3-2 regulations in Class D at 230 Vac multiplied by 230/110=2.09.

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