Power reduction of a 12-bit 40-MS/s pipeline ADC exploiting partial amplifier sharing

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***Abstract*—High performance analog-to-digital converters (ADC) are essential elements for the development of high performance image sensors. These circuits need a big number of ADCs to reach the required resolution at a specified speed. Moreover, nowadays power dissipation has become a key performance to be considered in analog designs, specially in those developed for portable devices. Design of such circuits is a challenging task which requires a combination of the most advanced digital circuit, the analog expertise knowledge and an iterative design. Amplifier sharing has been a commonly used technique to reduce power dissipation in pipelined ADCs. In this paper we present a partial amplifier sharing topology of a 12 bit pipeline ADC, developed in 0.35μm CMOS process. Its performance is compared with a conventional amplifier scaling topology and with a fully amplifier sharing one.**

Keywords- ADC, pipeline, CMOS, low-power

I. INTRODUCTION

Pipeline ADCs are popular architectures for high-speed data conversion (10-100 MS/s) at medium to high resolution (8-14 bits). They are employed in a variety of applications such as communications, imaging and instrumentation systems. Within this architecture, residue amplifiers are known to dominate power dissipation due to the simultaneous demand for low noise, high speed, and precise linear amplification. This is especially true for the amplifiers in the first few-stages of the pipeline, which have the greatest impact on the ADC overall performance.

Several techniques have been developed to reduce the power dissipation, although they are basically classified in two main types. One consists in reducing the power dissipation of the operational amplifiers. This can be achieved exploiting stage scaling techniques [1], where switched capacitor (SC) circuits in each stage are determined by noise requirements [2]. It has been proved that thermal noise contribution of a given stage is reduced by the previous stages gain. This allows the reduction of the capacitors size of that stage. The other technique is based on amplifiers sharing [3-5] between adjacent ADC stages working in opposite clock phases. This allows a theoretical reduction of one half in the number of amplifiers. However, amplifier sharing technique introduces some drawbacks since additional switches are needed in the implementation and thus, the series resistance is increased as well as the stage settling time.

On the other hand, the complexity of the pipeline stage is increased and more clock signals with different phases are needed for the switches of the ADC. The effect of the increased complexity on the power consumption is minimal compared to the benefit gained from the amplifier sharing if the ADC works with a resolution lower than 10 bits. However, an ADC with resolution higher than 10 bit and a big dynamic range could reduce the SNR or the bandwidth if amplifier sharing is used in the first stages, which makes that, in practice, the total power dissipation is only reduced one third of its initial value.

In this paper a hybrid amplifier sharing topology is proposed. The two first stages are designed as a conventional pipeline ADC, each one with its own amplifier, while the rest of stages take advantage of amplifier sharing technique. In this way we minimize some of the aforementioned drawbacks, specially the settling time for first stages. In order to evaluate the performance of the proposed topology, we have made a comparison with two equivalent converters: one of them has been built using fully amplifier sharing while the other one employs a single amplifier for each stage.

The structure of this paper is then the following. In section I we have presented the motivation of our work. Section II describes the topologies of the three different pipeline ADCs which are under study. The results obtained for the three topologies are described in section III. Finally we conclude in section IV.

II. STRUCTURES UNDER STUDY

In order to test the partial sharing technique, we have selected a 40-MS/s 12-bit pipeline ADC. It is composed by eleven stages working interleaved. They have a conversion schema of 1.5 bit per stage [6], and a Redundant-Signed-Digit architecture (RSD) to obtain the 12 bit output (Figs. 1, 4, 6). In each stage, the input signal is quantized by a flash ADC and then digitized again through a digital to analog converter (DAC). The difference between this last signal and the input one is multiplied by two and passed to the next stage.

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To obtain comparable results, we have analyzed three different topologies capable to achieve these specifications. The first one is a common topology without amplifier sharing. In the second topology all stages work with amplifier sharing technique. Finally the third topology is the one we propose, in which amplifier sharing is not used in the two first stages, while it is exploited in the rest of them.

A. Pipeline ADC without opamp sharing

This is the classical configuration of a pipeline ADC. In this configuration (Fig. 1) each stage has a Sample & Hold Amplifier (SHA) [7], which is composed of a switched capacitor circuit and operational transconductance amplifier (OTA). It can be demonstrated that *KT/C* noise contribution of a given stage is attenuated by the previous stages gain, which allows a scaling down of the sampling capacitors in latter stages without increasing the thermal noise significantly. Thus, in this ADC both the OTA and the sampling capacitors have been scaled depending on their position in the pipeline.

The last stage does not require amplification, and it consists only in the pair of comparators, working as a 2 bit flash ADC. Fig. 2 shows the structure of a single stage. The converter works in two semicycles. In the first one (Sample), the differential input signal ($Vin=V_{IN}^{+}-V_{IN}^{-}$) is applied, and the four capacitors $C_{s,f}$ are simultaneously charged to the input voltage. In the second semicycle (Amplify), the analog to digital converter starts to work. This converter consists of two differential dynamic comparators which quantize the signal with two bits of resolution. The outputs of the comparators are connected to the inputs of the DAC block which provide three voltage levels [8]. The DAC is an analog multiplexer with a digital decoder, whose analog output signal values can be: +Vref , 0 or –Vref, depending on the comparators output. The subtraction is done by connecting the bottom plate of each capacitor to the output of DAC with the values: +Vref = ($V_{REF}^{+}-V_{REF}^{-}$), 0 or -Vref = ($V_{REF}^{-}-V_{REF}^{+}$), and the operational amplifier passes the residue to the next stage which amplifies in a factor of two.

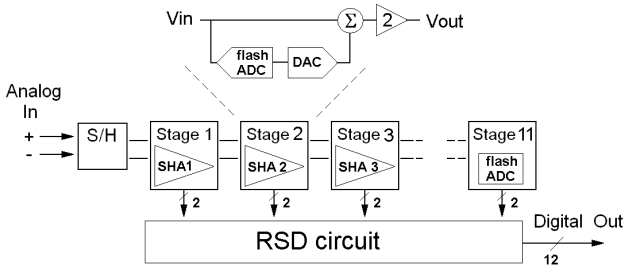
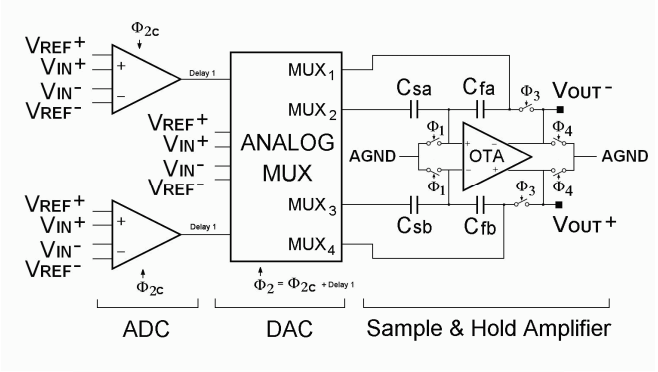


Figure 1. ADC with conventional scaling.



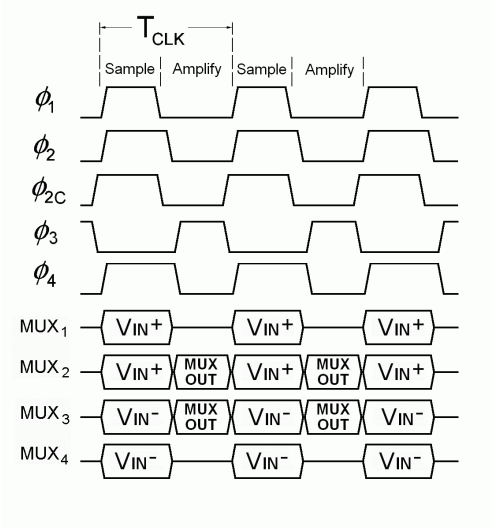


Figure 2. Single stage topology.

The transfer function of a single stage of the pipeline ADC is given by (1).

$$V_{out}=\left(1+\frac{C_{sa}}{C_{fa}}\right)V_{in}+\frac{C_{sa}}{C_{fa}}V_{ref} \tag{1}$$

where Cs = Cf and $Vout=V_{OUT}^{+}-V_{OUT}^{-}$. For the requirements of the ADC, we have chosen a telescopic operational amplifier with gain boosting [9]. The telescopic topology with gain boosting was chosen because it gives a high-dc gain, a high united gain bandwidth and a fast settling time. The circuit of the CMOS OTA with symmetrical input stage is shown in Fig. 3.

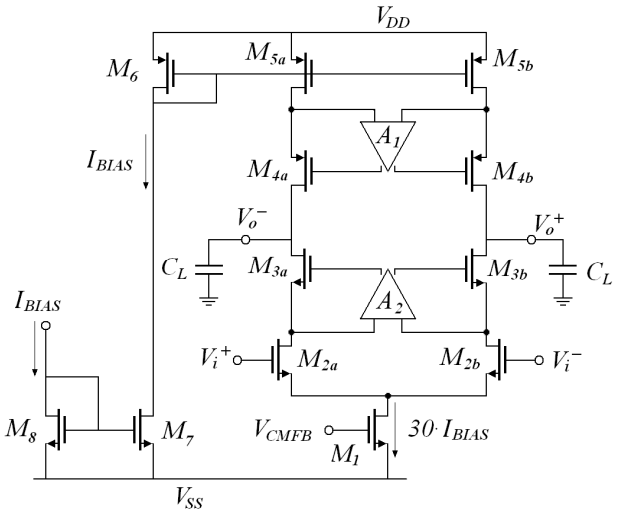


Figure 3. Fully Differential Telescopic CMOS OTA with gain boosting.

Transistor M_1, acts as a current source and is connected to a common mode feedback circuit (CMFB), which fixes the output common mode voltage to 1.8 V. The CMFB used is a switched capacitor configuration with symmetric loading of the differential loop [10]. This circuit settles much faster than other CMFB implementations, although it does not provide common mode control during the nonoverlap period of control clock signals. In the amplifier, the cascode transistors (M_3 and M_4) are used to get a high output resistance and increase the gain. The performance of the OTA used is shown in Tab. I

Although this ADC has been designed scaling down the sampling capacitors and the amplifiers of the latter stages, the design is not optimal in power dissipation because every amplifier is always working, independently of the clock semicycle.

TABLE I. EXTRACTED PRC SIMULATION RESULTS

Opamp Specification	Value
DC Gain (dB)	85.4
GBW (MHz)	570
PM (degree)	85.6
SR (V/μs) Closed loop	832
C_L (pF)	1.4
0.012% Settling (ns)	8.6
Current (mA)	4.8
Input / Output common mode	1.2 / 1.8
Power Supply	3.3

B. *Pipeline ADC with opamp sharing*

Fig. 4 shows the general topology of the ADC, whose stages have been designed using the amplifier sharing technique. With this topology, the number of OTAs is divided by two obtaining a reduction of the power dissipation but adding a complex circuit in the critical stages. The main difference regarding to a common stage is found in the SHA circuit. This circuit has been simplified and the OTA in Fig 2. has been removed, being now shared between adjacent stages. Thus, every stage contains now the comparators and the SC circuit. The size of the switches at the input of the operational amplifier (Fig. 2), the switches to drive signal to the i^{th} amplifier (Fig. 4) and the pair differential of the shared OTA are critical to get the required SNR.

The property of the successive pipeline stages working in opposite clock phases can be exploited by sharing the operational amplifier although this technique increases the complexity of the pipeline stages. Fig 5 shows a schematic of two sequential stages sharing the same operational amplifier.

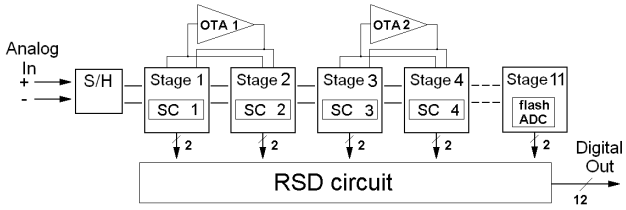


Figure 4. ADC with amplifier sharing.

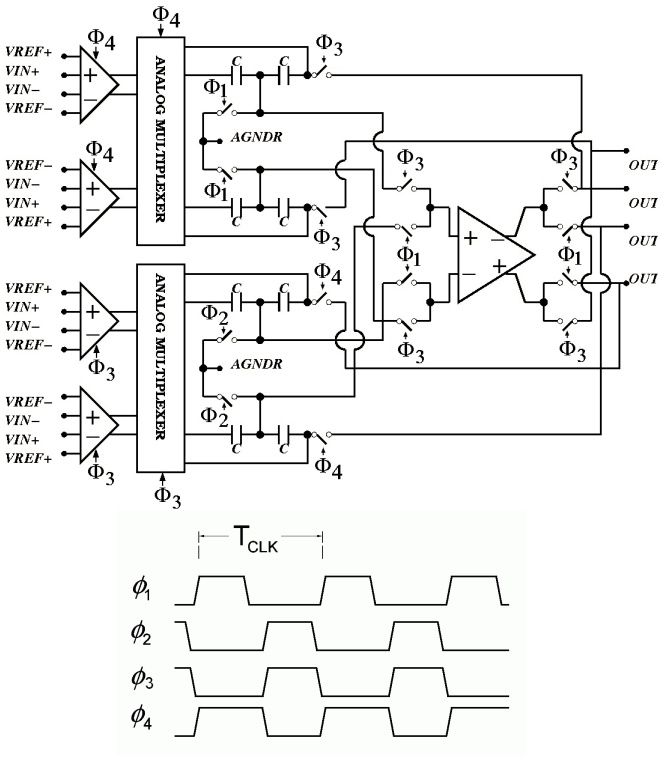


Figure 5. Structure of two stages with opamp sharing.

C. *Pipeline ADC with partial opamp sharing*

An ADC with resolution higher than 10 bit and a big dynamic range could reduce its SNR or bandwidth if amplifier sharing is used in the first stages. Three important side effects cause the reduction these parameters. First, the increased load capacitance of the amplifier affects the bandwidth requirement of the amplifier, which can be taken into account in the simulations. Second, the nonzero input voltage of the amplifier is never reset, which causes every sample to be affected by the finite gain error from the previous sample. This so-called memory effect can be tolerated with an adequate amplifier open loop DC-gain. Third, complex switch-capacitor circuits increase charge injection effects and reduce SNR. As the concept of amplifier sharing turns the ADC into a time-interleaved array, also the general performance limitations of pipeline ADCs must be considered.

In order to minimize the mentioned drawbacks, a mixed topology has been proposed, where amplifier sharing is applied to the stages 3 to 10, while the two first and more critical stages work with their own SHA circuits (Fig. 6). So, the number of OTAs is reduced keeping a robust design according to parameter as SNR and bandwidth. This topology is focused to minimize effects of additional circuitry in the two first stages, which are the most critical ones. These two stages have also a SHA scaled circuitry and their structure is similar to that show in Fig. 2. Topologies and connections of rest of the stages are the same than those used for the previous circuit.

III. RESULTS

A prototype of the ADC based on the first architecture without amplifier sharing was fabricated in a 0.35 µm CMOS technology (Fig. 7) [11]. The topology with full amplifier sharing has been designed just to obtain comparative results (Fig 8), and at the moment of writing this paper this amplifier was not prototyped. Finally, a prototype of the mixed topology has been recently manufactured (Fig 9), and the measurements in laboratory have not yet been performed.

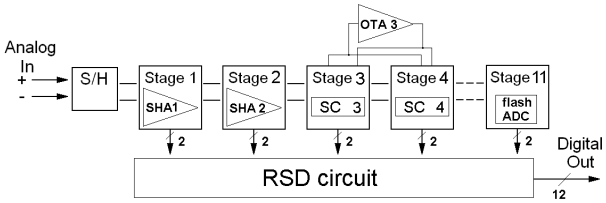


Figure 6. ADC with partial amplifier sharing.

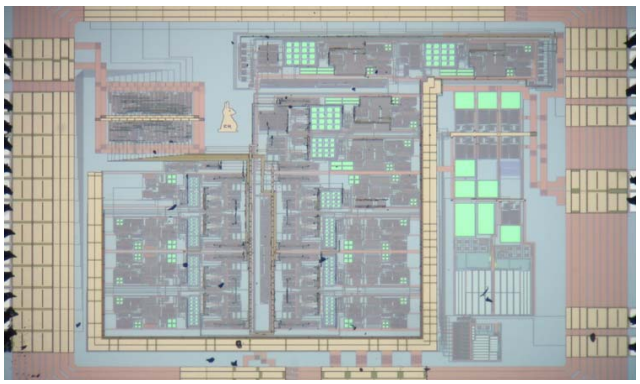


Figure 7. Chip microphotograph of the ADC without amplifier sharing.

Thus, in this paper, in order to offer comparable measurements, we show the results of the simulations with the parasitic resistors and capacitor (PRC) extractions from the three topologies.

In the three topologies, the technology employed has been AMS CMOS-C35B4 [12]. All the input and feedback capacitors have been scaled according to thermal noisy, number of bit and dynamic range. For every circuit, there is a generator of clock signals. The bias circuit generator controls and provides all bias currents of the ADC which can be generated from an internal or external master bias current. The RSD algorithm was implemented inside the three ADCs. Besides, the stability of the OTAs, bandwidth and DC-Gain were evaluated through extracted PRC simulations. The telescopic topology was implemented because it reached better results in phase margin and bandwidth than the other topologies as folded cascode when an identical power and capacitance load were used.

Results obtained from PRC extracted simulations of the three ADCs are shown in Tab II. They were obtained using IEEE Std 1241-2000, for a 4-parameter sine wave test which was implemented in ADCTEST software for MATLAB [13].

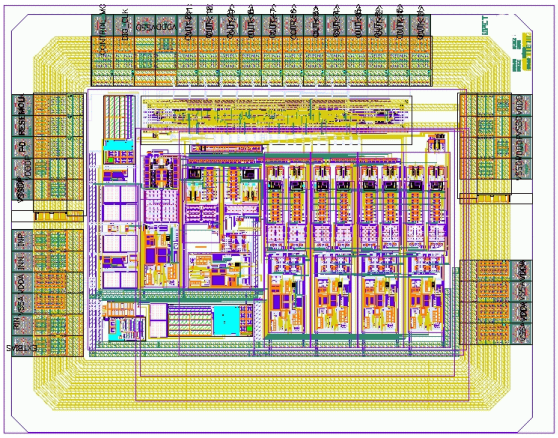


Figure 8. Layout of the ADC with full amplifier sharing.

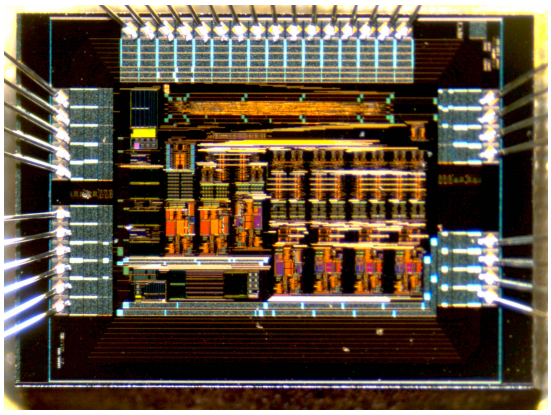


Figure 9. Chip microphotograph of the ADC with partial OTA sharing.

TABLE II. EXTRACTED PRC SIMULATION RESULTS

	Type of ADC		
	ADC1 No sharing	***ADC2 Full sharing***	***ADC3 Partial sharing***
SNDR (dB)	68.1	66.6	68.7
ENOB	11.06	10.81	11.16
Dynamic Range(Vpp)	3	3	3
Power (mW)	160.9	92.4	107
Linearity error (LSB)	+0.92 / -1.04	+1.77 / -1.2	+1.26 / -0.92
Size (mm2)	2.26 x 2.54	1.87 x 2.46	1.87x 2.46

All three circuits require the same power supply (3.3 v) and have been designed for input and output common mode voltages of 1.8 v. The input frequency has been 7 MHz and the sampling frequency has been 40 MS/s for the three circuits.As we can see, although the three ADCs offer a similar Signal plus Noise Distortion Ratio (SNDR), ADC3 presents the best relation between SNDR and power consumption. Moreover, ADC3 presents a higher robustness because of this uses a simplified circuitry in the first stages. This effect can be seen studied measuring the linearity error of the first stages of each ADCs. The first stage of ADC1 and ADC3 has a similar linearity error but this error is almost twice in ADC2. It means that in a typical simulation the results SNDR would be quite similar. However, small distortions could affect seriously the SNDR of ADC2 because it is working on the edge of the maximum error.

IV. CONCLUSIONS

We have presented a comparison of three topologies of pipeline ADCs. The first one is a common topology without amplifier sharing but with scaled operational amplifiers and capacitors. In the second topology all stages work with amplifier sharing technique and finally the third one, amplifier sharing is not used in the two first stages. All the OTAs used in the three ADCs are Fully Differential Telescopic circuits with gain boosting and common-mode feedback switched capacitor circuits inside (CMFB). This topology shows a high DC-Gain, a high united gain bandwidth and a fast settling.

The main drawback of amplifier sharing technique comes for the complex circuitry introduced in the design. The switches employed increase series resistance, which yield a higher settling time for each stage. This effect is especially important for the first stages, which are the more critical one in order to achieve required SNR or bandwidth. For this reason, a mixed topology using stage scaling for the first stages, and classical amplifier sharing for the latter ones has been developed. Although the lower power dissipation is achieved employing the amplifier sharing techniques in all the stages of the circuit, the partial amplifier sharing, applied to the latter stages of the circuit exhibits a good tradeoff between circuit resolution and power dissipation. At the present moment, we have not performed laboratory measurements of the prototype of the partial OTA sharing circuit. However, results obtained from extracted parasitic simulations show a good performance of this circuit. Although we expect some performance degradation mainly due to the increase of switches in the circuit, we think the measurements of the prototyped circuits will validate these initial results.

REFERENCES

[1] T. Cho and P. R. Gray, "A 10 b, 20 MSample/s, 35 mW pipeline A/D converter", IEEE J. Solid-State Circuits, vol. 30, no. 3, pp. 166-172, Mar. 1995.

[2] D. Cline and P. Gray, "A power optimized 13-b 5-Msamples/s pipelined analog-digital converter in 1.2μ CMOS", IEEE J of Solid State Circuits, vol. 31, pp-294-303, Mar. 1996.

[3] P. C. Yu and H.-S. Lee, "A 2.5-V, 12-b, 5-Msample/s pipelined CMOS ADC", IEEE J. Solid-State Circuits, vol. 31, no. 12, pp. 1854-1861, Dec. 1996.

[4] B. M. Min, P. Kim, F. W. Bowman, D. Boisvert and A. J. Aude, "A 69-mW 10-bit 80-MSample/s pipelined CMOS ADC", IEEE J. Solid- State Circuits, vol. 38, no. 12, pp. 2031-2039, Dec. 2003.

[5] D. Kurose, T. Ito, T. Ueno, T. Yamaji and T. Itakura, "55-mW 200-MSPS 10-bit Pipeline ADCs for Wireless Receiver", IEEE J. of Solid State Circuits, vol. 41, num. 7, July 2006.

[6] A. M. Abo and P. R. Gray, "A 1.5 V, 10-bit, 14-Msample/s CMOS Pipeline Analog-to Digital Converter". IEEE Journal of Solid State Circuits, Vol. 34, No 5. May 1999.

[7] R. J. Baker, "CMOS mixed-signal circuit design", Wiley-Interscience, 2002.

[8] L. Sumanen, Pipeline Analog-to-Digital Converters for Wide-Band Wireless Communications, PhD Diss., Helsinki Uni. of Tech. 2002.

[9] W. Jin and Q. Yulin, "Analysis and design of fully differential gainboosted telescopic cascode opamp", IEEE J. Solid State Circuits, vol.2, no. 18-21, pp. 1457-1460, Oct. 2004.

[10] O. Choksi and L. R. Carley "Analysis of Switched-Capacitor Common-Mode Feedback Circuit", IEEE Transactions on Circuits and Systems II, vol. 50, no. 12, pp 906-917. Dec. 2003.

[11] J.A. Diaz, H. Neubauer, G. Domenech and R. Ruiz "Comparative analysis of two operational amplifier topologies for a 40MS/s 12-bit pipelined ADC in 0.35μm CMOS", Intl. Conf. on IC Design and Technology, ICICDT 2008, Grenoble, France. 2-4 june, 2008.

[12] AustriaMikroSysteme, AG.

[13] J. Markus and I. Kollar, "Standard framework for IEEE-STD-1241 in MATLAB [ADC testing]" Procs. of the 18th Instrumentation and Measurement Technology Conf., 2001 Vol. 3, pp 1847-1852. May 2001.