Optimizing the Design of Single-Stage Power-Factor Correctors

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***Abstract*—This paper presents a new analytical method for the generalized study of a cluster of single-stage power-factor correctors (S^2PFCs). Due to this generalized approach, new topologies have been obtained, and the study of other known topologies has been simplified. The new analytical method simplifies the design of S^2PFCs by making it possible to compare a large number of different designs from the same viewpoint in order to identify the best topology. Finally, this research has enabled us to reduce the total size of the additional inductors that are used by a factor of two to three with respect to previous implementations.**

***Index Terms*—Current harmonics, IEC 61000-3-2 regulations, nonlinear loads, power-factor correction (PFC).**

I. Introduction

In order to reduce the low-frequency current harmonic content of ac-to-dc converters, regulation IEC 1000-3-2 (now IEC 61000-3-2) was published in 1995 [1]. Although unity power factor is the ideal objective, it is not an essential requirement to comply with the regulations. This fact has prompted the publication of numerous papers in the last few years, proposing nonsinusoidal solutions that offer advantages over the ideal unity-power-factor solution (sinusoidal). Because of their low cost, efficiency, and small size, nonsinusoidal solutions have been considered by several authors to be the best choice for low-power applications (up to 300 W, approximately) [2], [3]. Traditionally, two different paths have been followed to arrive at these solutions: 1) combining topologies (boost integrated flyback rectifier/energy storage dc/dc (BIFRED), charge pump, etc.) and 2) introducing minor modifications in the dc-to-dc converter (i.e., additional resonant output, input-current shapers, additional forward output, additional input) [2]. Nevertheless, some of these solutions have drawbacks. For example, a problem has been reported concerning BIFRED (one of the first proposals): the bulk capacitor voltage is very high and load dependent, so that the converter must work in discontinuous-conduction mode (DCM) or change the switching frequency [4]. In addition, since the latest changes in the regulations (where the classification "mask" has disappeared), some solutions have lost part of their initial interest [5].

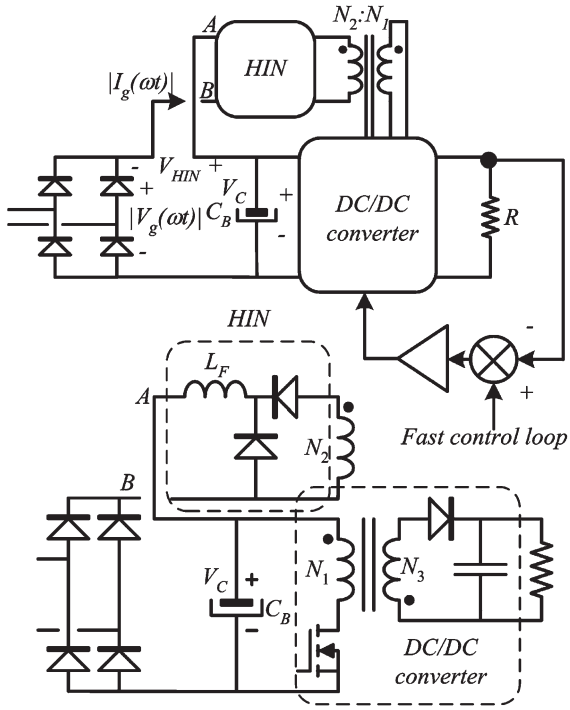

Fig. 1. S^2PFC general scheme.

However, the number of possible nonsinusoidal solutions is still large enough to make it difficult to choose the best option.

Many topologies that were derived from modifications on the dc-to-dc converter (with a boost as power-factor corrector) [6]–[11] can also be achieved by placing a high-impedance network (HIN) between the input rectifier and the dc-to-dc converter's bulk capacitor. Fig. 1 shows where a HIN must be placed and how it can be represented in a more general scheme. Due to this coincidence, it is possible to devise a common method for studying a large group of nonsinusoidal line-current solutions, thus facilitating the design of a single-stage power-factor corrector (S^2PFC). Due to the common origin of the solutions, the effect of small modifications on the topology configuration is easy to judge intuitively. In this way, nine S^2PFCs have been compared according to the HIN configuration. The studied HINs are based on the use of one additional converter output with either half-wave or full-wave rectifiers and one or two inductors.

II. HINs Based on Forward-Type Outputs

An extra winding that is coupled to a magnetic device is enough to obtain square-wave voltages in a dc-to-dc converter.

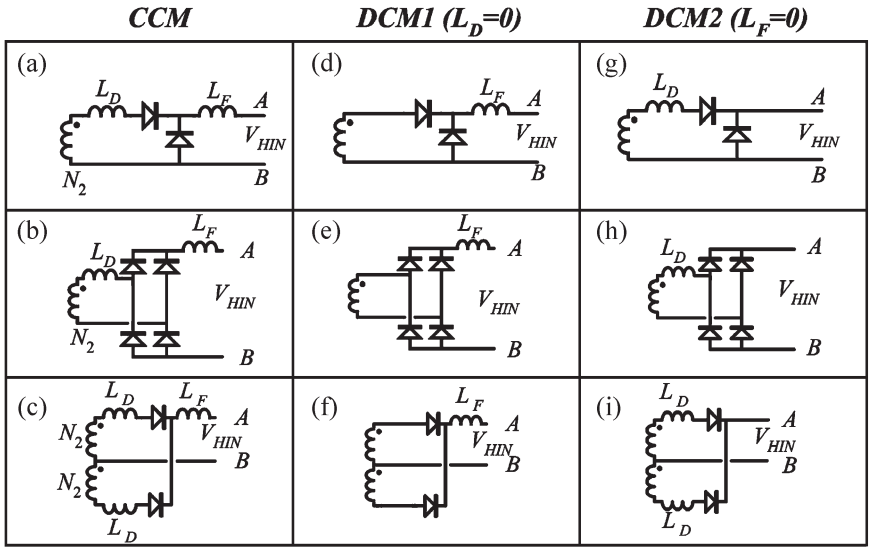

Fig. 2. HINs based on several forward-type outputs.

This square voltage can be rectified and filtered. The solution that is shown in Fig. 2(d) is produced using a half-wave rectifier (this topology was presented in [10]). In the same way, using a full-wave rectifier, topologies such as the ones that are shown in Fig. 2(e) and (f) can be produced. However, these topologies are not very useful because they only have high impedance in DCM. A new inductor "L_D" that is placed between the extra winding and the high-frequency rectifier can give the HINs in Fig. 2(e) and (f) the added attribute of high impedance in continuous-conduction mode (CCM) as well. In this way, the topologies shown in Fig. 2(a)–(c) can be achieved [7]–[9]. In order to look for new HIN topologies, filter inductor "L_F" can be removed, which would give the HINs in Fig. 2(g), (h), and (i). The solution in Fig. 2(g) was presented in [10] as the "magnetic switch" and in [12] as the "bus-voltage feedback." High-frequency diodes are not necessary in these solutions, given that the filter inductor works in DCM and there is an input rectifier with fast diodes (see Fig. 3). The solution in Fig. 2(i) was proposed in [11] for topologies with symmetrically driven transformers (half-bridge). In this paper, the HIN in Fig. 2(i) was tested coupled to the flyback inductor. Finally, the HIN in Fig. 2(h) can be coupled to any symmetrically driven converter transformer or to any converter inductor. Full-wave HINs cannot be used coupled to the transformer of a forward converter because this transformer is asymmetrically driven. Due to the different possibilities of coupling the HIN to the converter and of choosing the rectifier type, there are numerous possible solutions that can be studied with this method. Moreover, new solutions such as the HINs in Fig. 2(h) and (i) (in this case, coupled to the flyback inductor) have been obtained following this method.

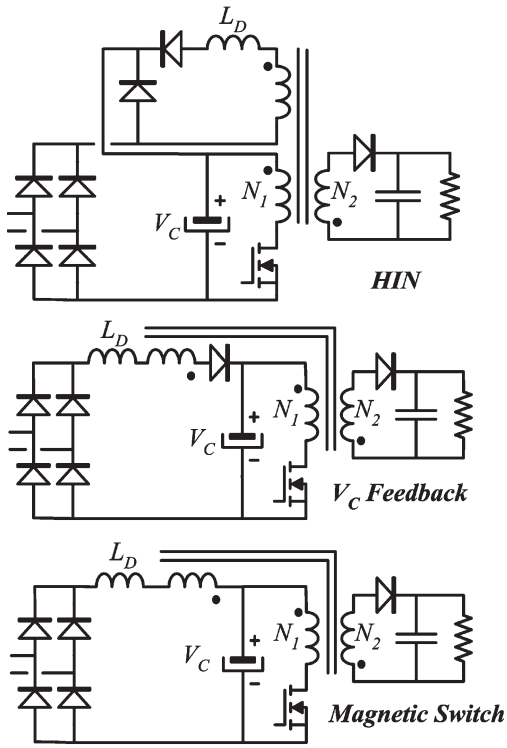

Fig. 3. Different approaches but same solution.

III. Input-Current Shape for Different HINs That Are Used in S^{2}PFCs

In order to obtain the input-current shape, the following assumption has been made: the bulk capacitor C_B is so big that its voltage can be considered constant during half of a line cycle. Therefore, the duty cycle in CCM is also constant. In these conditions, when the line rectifier is conducting, the voltage across the HIN ($V_{\rm HIN}$ in Fig. 1) can be calculated as the difference between the voltage across the bulk capacitor V_C and the rectified line voltage $|V_g(\omega t)|$. Thus, to calculate input current $I_g(t)$, the current flowing across the HIN $I_{\rm HIN}$ must be expressed as a function of $V_{\rm HIN}$. This function will be called the "voltage–current characteristic (VCC)." Two different VCCs will be used. One of these graphs connects the per-switching-cycle average value of the current flowing across the HIN with the applied voltage $V_{\rm HIN}$ and is used to calculate the input-current harmonic content. The second one connects the

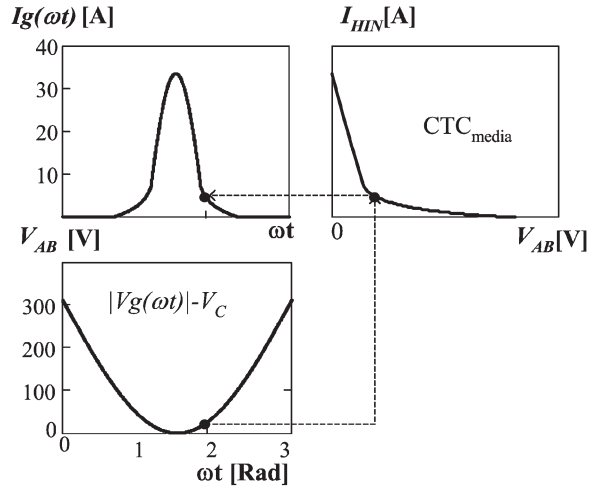

Fig. 4. How to obtain input current I_g from $V_{\rm AB}$ and VCC.

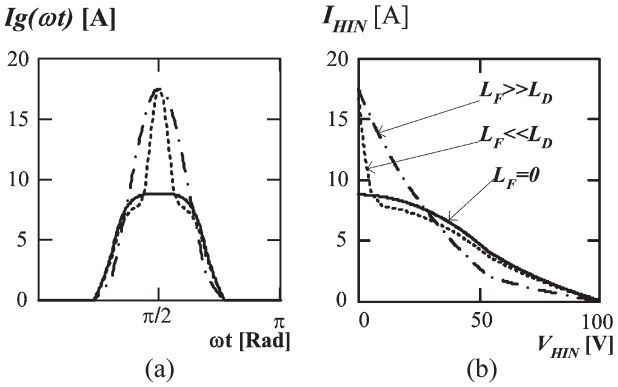

Fig. 5. (a) Input-current shapes for (b) different VCCs.

per-switching-cycle peak current with $V_{\rm HIN}$ and is used to assess the current stress. Fig. 4 shows how the VCC (per-cycle average current) can be used to obtain the input-current shape from $V_{\rm AB} = V_C - |V_g(\omega t)| = V_{\rm HIN}$. Several examples of the line-current shapes that were produced with the same HIN [Fig. 2(b)] are shown in Fig. 5(a). In this example, L_D is maintained to be constant, and L_F is different for each VCC. As the curves show in Fig. 5, the input-current shape may be different for the same HIN topology but with a different inductor ratio. In this way, S^2PFC analysis can be simplified by using the HIN and VCC concepts. However, some important issues must be taken into account. Thus, the number of conduction modes is different in comparison with the ones of a standard dc-to-dc converter. A standard dc-to-dc (e.g., buck) can operate either in CCM or DCM. Nevertheless, HINs with L_D and L_F have several DCMs and CCMs. A detailed study of all the HINs must be done to determine the different conduction modes, the limits among them, and the current and voltage waveforms.

IV. Example of Calculating the VCC for a Specific HIN

The chosen example is a full-wave-rectifier HIN that is coupled to a flyback inductor (see Fig. 6). The voltage applied across the winding N_2, as well as a detailed description of the selected HIN, are shown in Fig. 7. Assuming that the flyback

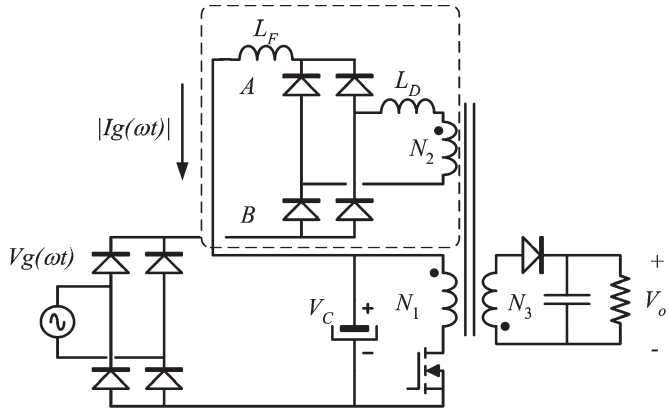

Fig. 6. Converter example.

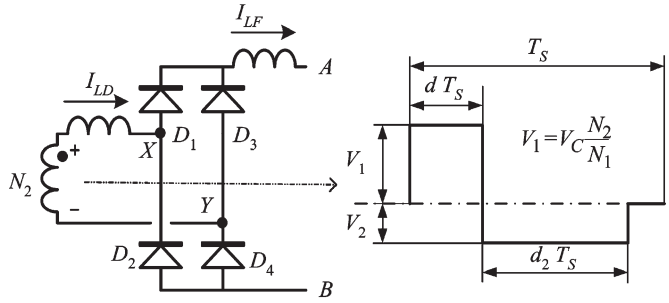

Fig. 7. Voltage shape across winding N_2.

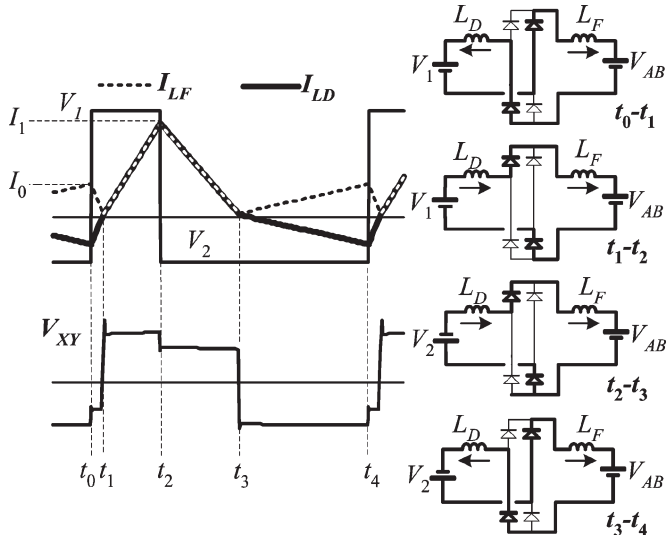

Fig. 8. Operation mode 1.

inductor is in CCM and the maximum duty cycle is 0.5, the HIN includes six different operation modes.

A. Operation Mode 1 (Fig. 8)

This mode appears under the following conditions:

$$V_{\rm AB} > V_1 \frac{L_F}{L_D}, V_{\rm AB} > V_2 \frac{L_F}{L_D}$$

and L_F is in CCM.

In order to obtain the line-current shape, which is the same as $I_{\rm LF}$, four unknown quantities I_0, I_1, t_1, and t_3 (see Fig. 8) must be calculated; thus, four equations are required. These equations can be deduced from the HIN's behavior over different time intervals.

1) Interval t_0–t_1: In the equivalent circuit that is shown in Fig. 8, only bold diodes are conducting; therefore, the inductors are in series. Thus, the initial current in L_F (I_0) can be calculated as follows:

$$\frac{V_1 + V_{\rm AB}}{L_F + L_D} t_1 = I_0. \tag{1}$$

2) Interval t_1–t_2 (Where $t_2 = dT_s$): Whenever the current across L_D is zero, conducting diodes change, and the inductors voltage is modified. Filter inductor peak current I_1 is calculated as

$$\frac{V_1 - V_{\rm AB}}{L_F + L_D}(t_2 - t_1) = I_1. \tag{2}$$

3) Interval t_2–t_3: The inductors are still in series (the same diodes are ON); however, the transformer voltage changes, so the current slope is modified as shown by

$$\frac{V_2 + V_{\rm AB}}{L_F + L_D}(t_3 - t_2) = I_1. \tag{3}$$

4) Interval t_3–t_4 (Where $t_4 = t_s$): The last current value must be the same as the first one. This gives

$$\frac{V_2 - V_{\rm AB}}{L_F + L_D}(t_4 - t_3) = I_0 \tag{4}$$

and the equation system is completed.

I_0, I_1, t_1, and t_3 can be obtained by solving the equation system given by (1)–(4). Voltage $V_{\rm XY}$ (see Fig. 7) can be used to check the conducting diodes.

B. Operation Mode 2 (Fig. 9)

This mode appears under the following conditions:

$$V_{\rm AB} < V_1 \frac{L_F}{L_D} \quad V_{\rm AB} > V_2 \frac{L_F}{L_D}$$

and L_F is in CCM.

As shown in Fig. 9, there are five unknown quantities (I_0, I_1, I_2, t_1, and t_3); thus, five equations are required. Again, these equations can be calculated from the HIN's behavior during different time intervals.

1) Interval t_0–t_1: During this period of time, all diodes are conducting $(V_{\rm XY} = 0)$. In these conditions, the voltage applied across each inductor is different; thus, the following can be derived from this interval:

$$\frac{V_1}{L_D} t_1 - I_0 = I_1 \tag{5}$$

$$I_0 - \frac{V_{\rm AB}}{L_F} t_1 = I_1. \tag{6}$$

This period ends when $I_{\rm LD}$ reaches $I_{\rm LF}$.

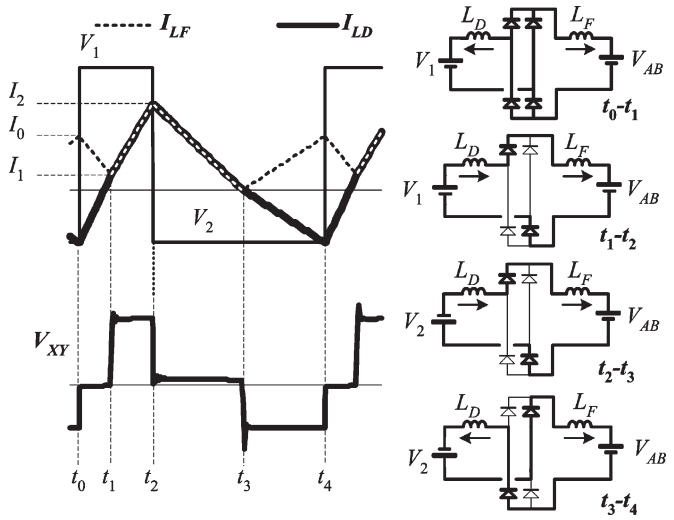

Fig. 9. Operation mode 2.

2) Interval t_1–t_2 (Where $t_2 = dT_s$): During this interval, only D_1 and D_4 are conducting; thus, the inductors are in series, and only one equation can be obtained, i.e.,

$$I_1 + \frac{V_1 - V_{\rm AB}}{L_F + L_D}(t_2 - t_1) = I_2. \tag{7}$$

3) Interval t_2–t_3: This interval is similar to the same period in operation mode 1. Hence, the following is equivalent to (3):

$$\frac{V_2 + V_{\rm AB}}{L_F + L_D}(t_3 - t_2) = I_2. \tag{8}$$

4) Interval t_3–t_4 (Where $t_4 = t_s$): Two diodes are conducting, and so, only

$$\frac{V_2 - V_{\rm AB}}{L_F + L_D}(t_4 - t_3) = I_0 \tag{9}$$

can be obtained.

I_0, I_1, t_1, and t_3 are deduced from the system of equations given by (5)–(9).

C. Operation Mode 3

This operation mode would appear if $V_{\rm AB} > V_1(L_F/L_D)$ and $V_{\rm AB} < V_2(L_F/L_D)$. Nevertheless, these conditions are impossible because the maximum duty cycle is 0.5.

D. Operation Mode 4 (Fig. 10)

This mode holds when $V_{\rm AB} < V_1(L_F/L_D)$, $V_{\rm AB} < V_2(L_F/L_D)$, and L_F is in CCM.

To calculate the peak and average currents across L_F in this operation mode, six unknown values must be calculated (I_0, I_1, I_2, I_3, t_1, and t_3). As in previous operation modes, different equations will be derived from each interval.

1) Interval t_0–t_1: This period is equivalent to interval t_0–t_1 of operation mode 2, and so, the associated equations are (5) and (6).

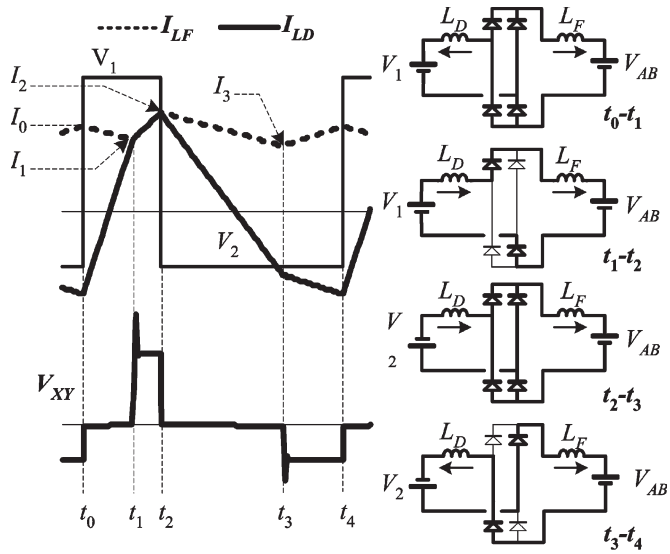

Fig. 10. Operation mode 4.

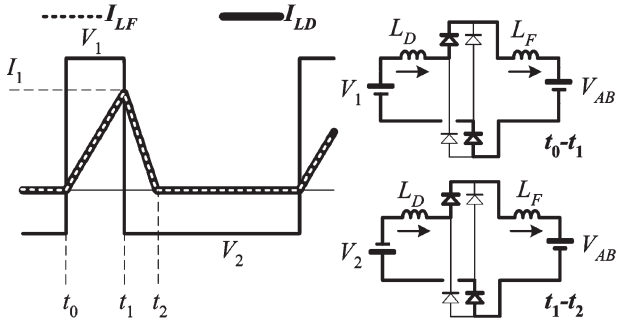

Fig. 11. Operation mode 5.

2) Interval t_1–t_2 (Where $t_2 = dT_S$): This period is equivalent to interval t_1–t_2 of operation mode 2, and so, the associated equation is (7).

3) Interval t_2–t_3: The four diodes are conducting ($V_{\rm XY} = 0$), so the associated equations are

$$\frac{V_2}{L_D}(t_3 - t_2) - I_2 = I_3 \tag{10}$$

$$I_2 - \frac{V_{\rm AB}}{L_F}(t_3 - t_2) = I_3. \tag{11}$$

4) Interval t_3–t_4 (Where $t_4 = t_s$): This interval begins when $I_{\rm LD}$ and $I_{\rm LF}$ have the same values. At that point, D_1 and D_4 switch off, and both inductors are in series. The associated equation is

$$I_3 + \frac{V_{\rm AB} - V_2}{L_F + L_D}(t_4 - t_3) = I_0. \tag{12}$$

I_0, I_1, I_2, I_3, t_1, and t_3 can be found by solving the equation system given by (5)–(7) and (10)–(12).

E. Operation Mode 5 (Fig. 11)

This mode holds when $V_{\rm AB} > V_2(L_F/L_D)$ and L_F is in DCM.

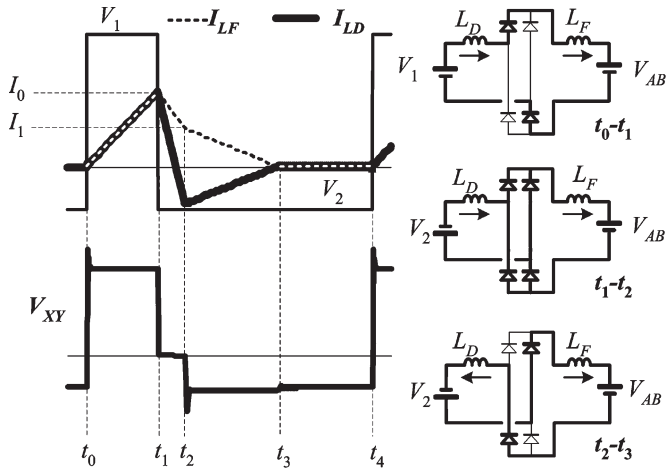

Fig. 12. Operation mode 6.

1) Interval t_0–t_1 (Where $t_1 = dT_s$): The initial current is zero, so D_1 and D_4 are conducting. The peak current value can be calculated as

$$\frac{V_1 - V_{\rm AB}}{L_F + L_D} t_1 = I_1. \tag{13}$$

2) Interval t_1–t_2: Applying the volt-second balance, time t_2 is given by

$$\frac{V_2 + V_{\rm AB}}{L_F + L_D} t_2 = I_1. \tag{14}$$

F. Operation Mode 6 (Fig. 12)

This mode holds when $V_{\rm AB} < V_2(L_F/L_D)$ and L_F is in DCM.

Four equations are required to calculate I_0, I_1, t_2, and t_3.

1) Interval t_0–t_1 (Where $t_1 = dT_s$): This period is equivalent to interval t_0–t_1 of operation mode 5. Consequently, the associated equation is

$$\frac{V_1 - V_{\rm AB}}{L_F + L_D} t_1 = I_0. \tag{15}$$

2) Interval t_1–t_2 (Where $t_2 = dT_s$): During this interval, all diodes are conducting, and so, the following can be derived:

$$I_0 - \frac{V_{\rm AB}}{L_F}(t_2 - t_1) = I_1 \tag{16}$$

$$\frac{V_2}{L_D}(t_2 - t_1) - I_0 = I_1. \tag{17}$$

3) Interval t_2–t_3: When $I_{\rm LD}$ and $I_{\rm LF}$ are equal, D_1 and D_4 switch off. This period ends when $I_{\rm LD}$ becomes zero. Therefore, the interval equation is

$$\frac{V_{\rm AB} - V_2}{L_F + L_D}(t_3 - t_2) = I_1. \tag{18}$$

The HIN's input current (peak and average) can be calculated by solving the equation system given by (15)–(18).

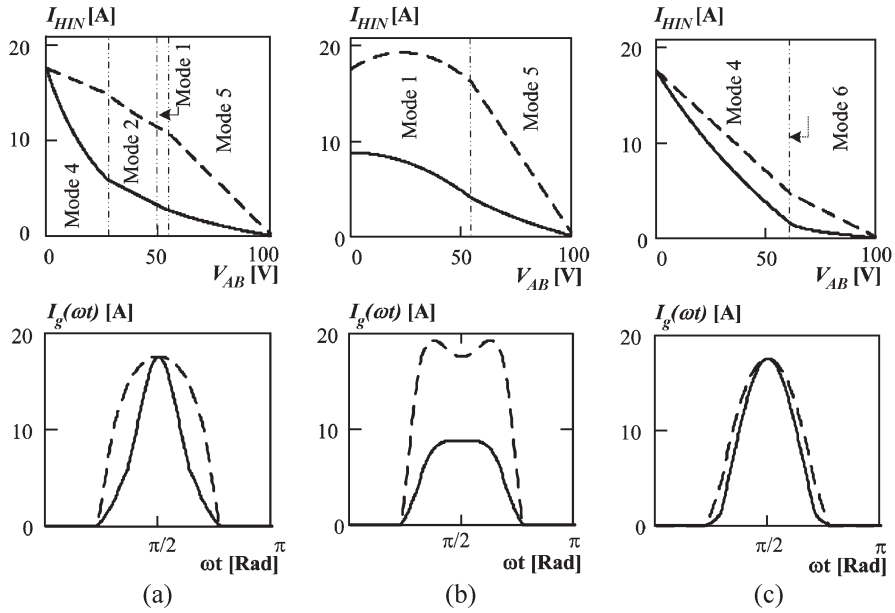

Fig. 13. VCC (peak and average) and input-current shapes (peak and average) for different inductor configurations. (a) $L_F/L_D = 0.5$, $L_D = 10$ μH, and $L_F = 5$ μH. (b) Only L_D, $L_D = 10$ μH, and $L_F = 1$ nH. (c) $L_F/L_D = 2$, $f_s = 100$ kHz, $L_D = 10$ μH, $L_F = 20$ μH, $d = 0.35$, and $V_1 = 100$.

Fig. 13 shows the different VCCs that were obtained from the previously derived equations. In this example, the input peak line voltage and the bulk capacitor voltage were assumed to have the same values. The dotted curves represent peak VCC and peak input current, and the solid curves represent average VCC and average input current. All the derived equations have both a filter inductor and a delayed inductor. Nevertheless, the HIN shown in Fig. 2(h) only has one inductor. To study this case, the L_F value must be negligible related to L_D [Fig. 13(b)]. Similarly, when there is only a filter inductor L_F, the L_D value must be also negligible.

V. Quality Parameters and Qualitative Evaluation of the HINs

In order to determine which HIN is the best from the design viewpoint, quality parameters must be established. In this sort of S^2PFC, there is no current loop for the input current, so the converter must itself adapt the input and output powers. This power regulation can be done in either of two different ways: 1) by changing the VCC or 2) by changing bulk capacitor voltage V_C. The change of V_C has greater effect, and it is the natural way that S^2PFC has to regulate the handled power. However, the increase of the voltage across the bulk capacitor has a negative effect in the converter design, and so, the maximum bulk capacitor voltage will be a quality parameter. Moreover, due to the fact that the dc-to-dc converter has to work with an additional load the HIN, it has an additional problem: The current stress increases. Therefore, the best topology must satisfy three conditions.

- The harmonic content of the input-current waveform must be below the limit that was specified in the regulations.
- The maximum bulk capacitor voltage should be as low as possible.
- The additional current stress in semiconductor devices that is caused by the HIN must also be as small as possible (note that the HIN is an additional output of the dc-to-dc converter).

Moreover, as Fig. 5 shows, input-current shapes depend on the selected HIN and the ratio between inductors L_F and L_D, which is defined as $K = L_F/L_D$. If several topologies have similar maximum bulk capacitor voltages, low output-voltage ripple, similar stress currents, and of course, harmonics that are below the regulation limits, then the configuration with the smallest magnetic component will be the best. In order to evaluate magnetic component sizes accurately, an electromagnetic interference (EMI) filter inductor must be included (at least approximately). Then, the inductor's stored energy will be another quality parameter, which must be as low as possible.

VCC can be a qualitative means of determining which HIN is the most suitable to be used as harmonic limiter. Fig. 14 shows both types of VCC [averaged (solid line) and peak (dotted line)] of the proposed HINs for different inductor configurations, with all of them designed for an S^2PFC where the dc-to-dc converter is a flyback. These VCCs have also been calculated with a half-bridge as dc-to-dc converter, with similar results. All the graphs that are shown in Fig. 14 were obtained with the same voltage shape applied across N_2, the same switching frequency, and the same value of L_D, except for the HIN without L_D (when there is only one inductor, it has the design value "L_D"). Examination of this figure produces three conclusions.

- Topologies without a "delaying inductor" $(L_D = 0)$ must avoid low-impedance zones (high slope). Therefore, to allow high-impedance operation, the bulk capacitor voltage must be higher than the peak line voltage plus the voltage that allows high impedance in the HIN. These topologies have the highest bulk capacitor voltages. Full-wave HINs

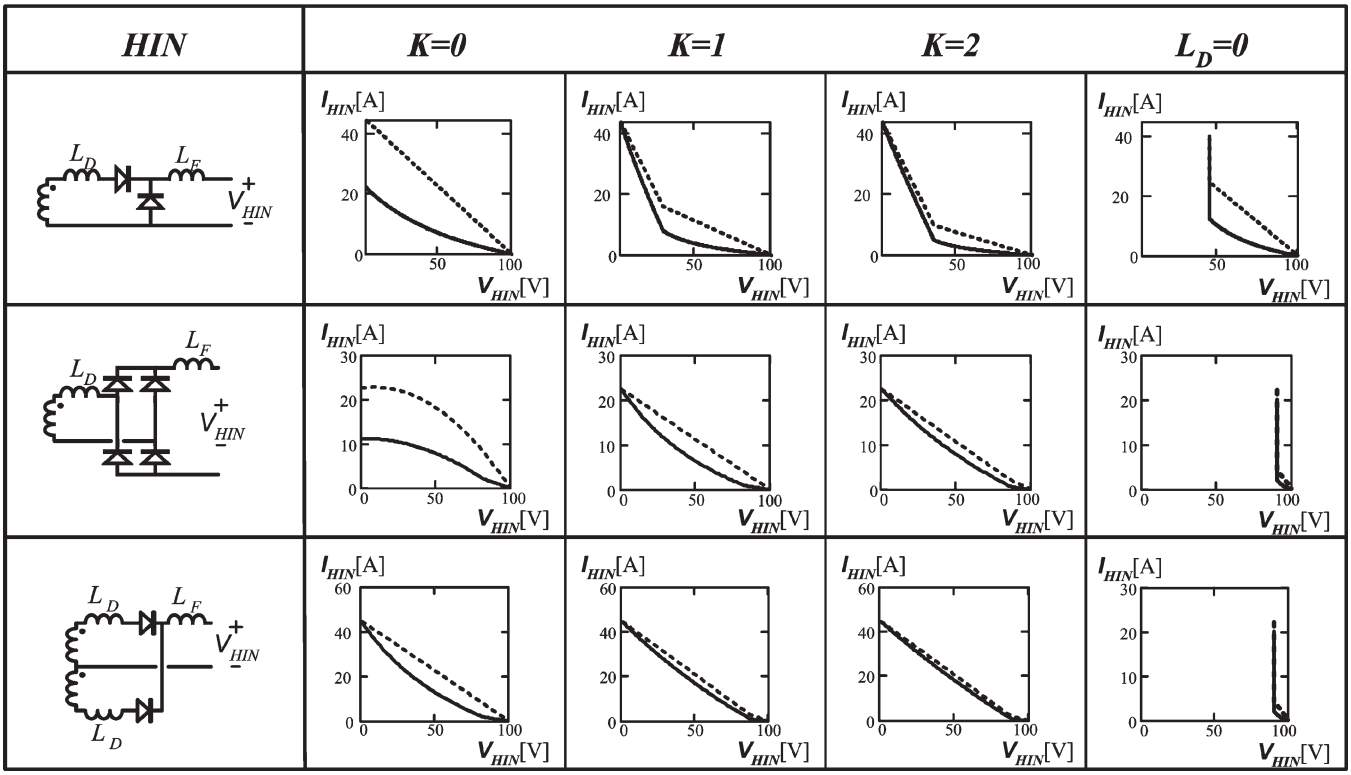

Fig. 14. (Dotted line) $\mathrm{VCC_{peak}}$ and (solid line) $\mathrm{VCC_{AVG}}$ for the HINs that are shown in the leftmost column.

without a "delayer inductor" present small intervals of high-impedance operation; therefore, topologies of this kind are a bad solution. Only half-wave topologies can be said to be useful.

- Topologies with two inductors [included in Fig. 2(i)] with both the value of the peak current and the average current coincide when V_{HIN} is zero. Current stress does not then increase appreciably when filter inductor L_F is reduced. It is estimated that the filter inductor size can be reduced further than that in previous solutions [8], [9].
- With the same value of L_D, the topology that is shown in Fig. 2(h) has the highest impedance, but the current stress is higher that in other cases.

VI. Design Examples: Quantitative Evaluation of HINs

In order to verify the preceding considerations on the design of an S^{2}PFC, different HINs were designed with the same specifications: flyback as dc-to-dc converter, 100 W, output voltage of 54 V, line voltage of 190–265 V_{rms}, Class D, maximum duty cycle $= 0.35$, switching frequency $= 100$ kHz, and $C_B = 47\ \mu$F. The maximum bulk capacitor voltage V_{Cmax} is reached within the limit between CCM and DCM for the maximum line voltage [4], [8], so, in order to include this parameter, this limit is fixed at 33 W. The minimum bulk capacitor voltage is reached with full load for the minimum line voltage; for topologies with two inductors, this value must be the minimum peak line voltage ($190\sqrt{2}V$ with the design specifications). All of these HINs were designed so that the most critical harmonic (the third one) was 5% below the limit

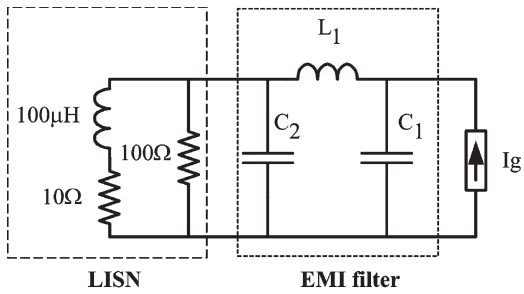

Fig. 15. EMI filter simplified equivalent circuit.

that was specified in the regulations. EMI filters were designed to comply with regulation CISPR22, and so, the EMI filter size is included in the quality assessment.

A simplified EMI design was made to assess the filter-inductor size. Moreover, only a differential-mode EMI filter has been evaluated. Fig. 15 shows the filter structure and the simplified linear-impedance-stabilization-network equivalent circuit [13]. In this example, C_1 and C_2 have the same values: 470 nF. This value was chosen in order to avoid any appreciable disturbance to the theoretical line-current waveforms. An inductor "L_1" was calculated for each design.

Parameter $\sum I_x^2 L_x/2$ was introduced to represent the total size of the magnetic devices that was used in the different HINs and the "L_1" filter inductor. This parameter represents the peak stored energy in the HIN's inductors and the EMI filter inductor. As the results that are given in Table I show, in several cases, the maximum bulk capacitor voltage and additional stress current I_{Speak} are very similar for different possible designs; therefore, they are not very representative. Nevertheless, the inductor-size

TABLE I
QUALITY PARAMETERS FOR DIFFERENT DESIGNS

HIN Fig.2.a	K=0	K=0.5	K=1	K=10
N_1/N_2	3.72	1.7	1.88	1.7
$L_D(\mu H)$	76	345	312	459
$L_F(\mu H)$	0	172	312	4590
$I_{HINpeak}(A)$	3.2	1.6	1.6	1.5
$\Delta I_{Speak}(A)$	0.86	0.94	0.85	0.88
$V_{Cmax}(V)$	423	437	413	413
$L_1(\mu H)$	2700	770	477	63
$\sum I_x^2 L_x/2(\mu J)$	3854	1647	1410	5750
HIN Fig.2.b	**K=0**	**K=0.5**	**K=1**	K=10
N_1/N_2	**4**	**3.17**	**2.9**	3
$L_D(\mu H)$	**47**	**87**	**107**	116
$L_F(\mu H)$	**0**	**44**	**107**	1160
$I_{HINpeak}(A)$	**2.7**	**1.7**	**1.5**	1.445
$\Delta I_{Speak}(A)$	**0.65**	**0.53**	**0.51**	0.47
$V_{Cmax}(V)$	**434**	**426**	**418**	416
$L_1(\mu H)$	**1860**	**980**	**560**	57
$\sum I_x^2 L_x/2(\mu J)$	**2860**	**1170**	**870**	1310
HIN Fig.2.c	K=0	K=0.5	K=1	K=10
N_1/N_2	2.89	2.89	2.99	2.89
$L_D(\mu H)$	215	228	224	245
$L_F(\mu H)$	0	114	224	2450
$I_{HINpeak}(A)$	1.5	1.4	1.4	1.3
$\Delta I_{Speak}(A)$	0.50	0.48	0.47	0.45
$V_{Cmax}(V)$	418	419	419	421
$L_1(\mu H)$	555	290	190	28
$\sum I_x^2 L_x/2(\mu J)$	1108	843	968	3340

parameter is strongly affected by the inductor configuration. As shown in Table I, the amount of stored energy in the full-wave HIN and its EMI filter is smaller than that in the half-wave HIN. Full-wave-HIN (and EMI filter) inductor sizes are therefore also smaller. In terms of the peak stored inductor energy that was shown in Table I ($\sum I_x^2 L_x/2$), the best HINs are given as follows:

- topology that is shown in Fig. 2(b) (full wave and four diodes) with $K = 1$;
- topology that is shown in Fig. 2(c) (full wave and two diodes) with $K = 0.5$.

TABLE II
QUALITY PARAMETERS FOR THE BEST SOLUTIONS

HIN Fig.2.b	K=0.75	**K=1.5**	**K=2**	K=3
N_1/N_2	2.99	**2.89**	**2.89**	2.89
$L_D(\mu H)$	99	**116**	**114**	114
$L_F(\mu H)$	75	**174**	**228**	324
$I_{HINpeak}(A)$	1.6	**1.5**	**1.4**	1.4
$\Delta I_{Speak}(A)$	0.53	**0.52**	**0.48**	0.48
$V_{Cmax}(V)$	421	**418**	**419**	419
$L_1(\mu H)$	710	**350**	**290**	200
$\sum I_x^2 L_x/2(\mu J)$	993	**723**	**711**	738

The value of the size quality parameter $\sum I_x^2 L_x/2$ of the four-diode HIN is strongly affected by the EMI filter inductor. Therefore, inductor size L_1 can be reduced by using bigger EMI filter capacitors. Nevertheless, the energy that is stored in the HIN inductors that is shown in Fig. 2(c) is an important contribution to the overall stored energy, and so, increasing EMI filter capacitors will not greatly improve the inductor-size parameter.

More results for the HIN that is shown in Fig. 2(b) are given in Table II. As shown, $K = 2$ is the best solution according to the selected quality parameters, without modifying the EMI filter capacitors (470 nF).

As shown in Table I, even with $K = 10$, a differential-mode EMI filter is necessary to comply with the EMI regulations ($L_1 \neq 0$). Therefore, instead of enlarging HIN filter inductor L_F, it is better to enlarge EMI filter inductor L_1. Note that only the differential-mode EMI filter is considered in this analysis. Of course, a common-mode filter will also be necessary.

VII. EXPERIMENTAL RESULTS

The inferences presented previously are based on a simplified study of the S^{2}PFC, where only the HIN is analyzed, instead of the complete converter. Thus, to verify the conclusions obtained as a consequence of this study, some experimental results that were obtained in a complete prototype (a complete S^{2}PFC) are presented in this section. It should be noted that there are simple models (based on the loss-free resistance concept [8]) that are very accurate for HINs with high values of K ($K \geq 2$). Nevertheless, the suggested design method is suitable for all values of K. Due to this, the HINs that were used in the prototype that is presented in this section have low values of K.

The prototype that is described in Section VI was implemented in the laboratory with different HINs (the ones that are shown in boldface in Table I with $K = 0$, $K = 0.5$, and $K = 1$).

Fig. 16 shows the oscillograms of input current I_g and line voltage ($V_g = 230\ V_{\rm rms}$) at full load for the studied HINs [Fig. 2(b)] at different values of K ($K = 0$ [Fig. 16(a)],

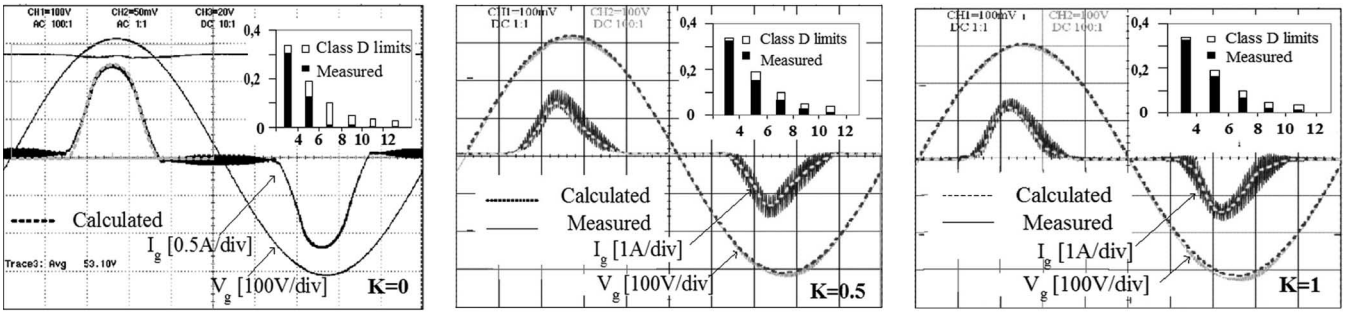

Fig. 16. (Dotted line) Calculated and measured input currents for (a) $K = 0$, (b) $K = 0.5$, and (c) $K = 1$, for $V_g = 230\ V_{\rm rms}$ and full load (100 W).

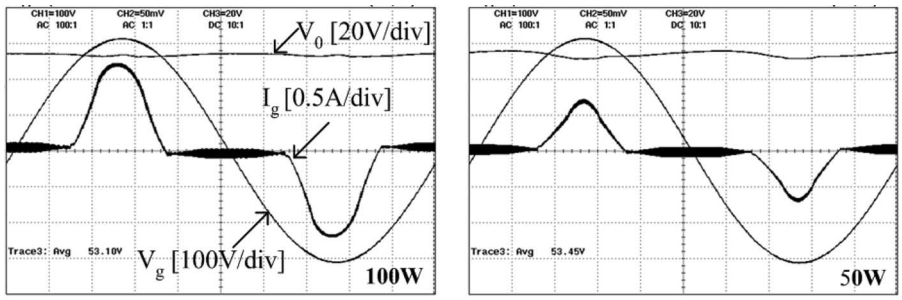

Fig. 17. Input current and output voltage without control loop for the line voltage (230 $V_{\rm rms}$) and $K = 0$. (a) Full load. (b) Half load.

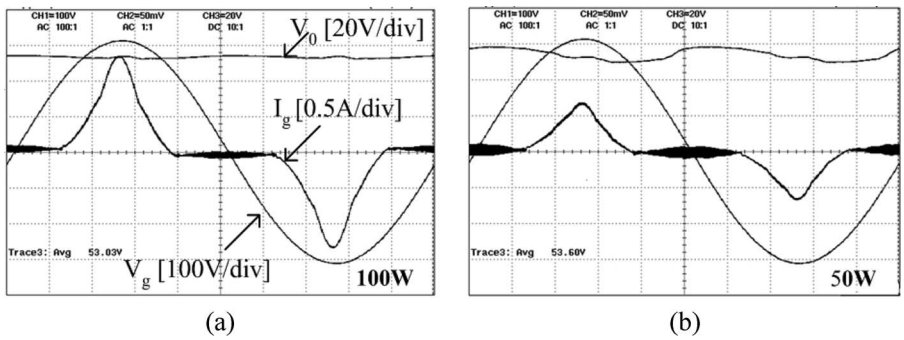

Fig. 18. Input current and output voltage without control loop for the line voltage (230 $V_{\rm rms}$) and $K = 0.5$. (a) Full load. (b) Half load.

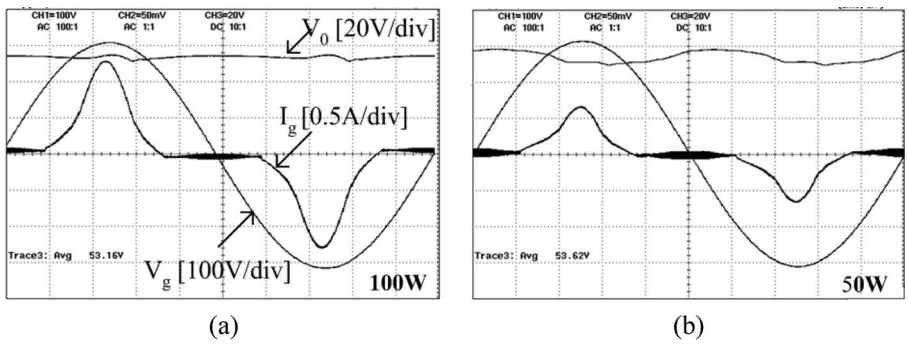

Fig. 19. Input current and output voltage without control loop for the line voltage (230 $V_{\rm rms}$) and $K = 1$. (a) Full load. (b) Half load.

$K = 0.5$ [Fig. 16(b)], and $K = 1$ [Fig. 16(c)]). It can be noted that the measured and calculated values (dotted lines) are in good agreement, and so, the current harmonic content is under the regulation limits within the predicted margin of safety.

In order to see how the output-voltage ripple is affected by the HIN current, the oscillograms that are shown in Figs. 17–19 have been obtained with a very slow voltage control loop. Although the voltage ripple increases for low loads, a high-frequency control loop can correct this perturbation [14].

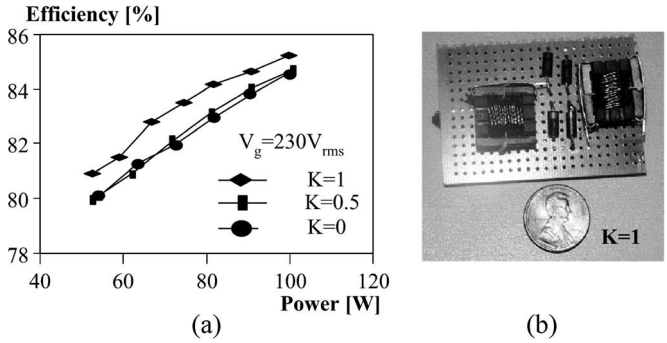

Fig. 20. (a) Efficiency for different configurations. (b) Additional elements (HIN inductors and diodes) that were added to comply with the regulations in a 100-W prototype for $K = 1$.

Fig. 20(a) presents the efficiency of the three prototypes, where it can be noted that HINs with higher current stress are subject to more losses ($K = 0$ and $K = 0.5$). Nevertheless, all the efficiencies are very similar.

The maximum voltage across the bulk capacitor that was reached in each case is 432 V for $K = 0$, 423 V for $K = 0.5$, and 417 V for $K = 1$.

The magnetic cores that were used in the prototype were the following: EE16 for L_D and EE12 for L_F (when $K = 0.5$), two EE16s for $K = 1$ [Fig. 20(b)], and one EE16 for $K = 0$. As can be seen, only small additional inductors are needed to comply with the regulations.

VIII. Conclusion

The proposed method makes it possible to analyze a large number of S^2PFCs from the same viewpoint, thus facilitating the design. Among the considered HINs, the optimum solution is the full-wave rectifier with four diodes and two inductors with similar values (with a conservative EMI filter design using small capacitors). In this way, the total size of the additional inductors that were used can be reduced by a factor of two to three with respect to previous implementations. In addition, new S^2PFCs have been produced, which use the HIN that is shown in Fig. 2(h) on full-bridge and half-bridge dc-to-dc converters and the HIN that is shown in Fig. 2(i) on flyback, Sepic, and Cúk dc-to-dc converters.

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