Effect of the Output Impedance in Multiphase Active Clamp Buck Converters

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***Abstract*—Passive current sharing in multiphase converters, where resistive losses are not dominant, is a quite complex goal. In this paper, an averaged model of an active clamp buck converter was obtained. It has been checked that this topology presents high output impedance. This property is used like a lossless passive equalization. The principle of operation, theoretical analysis, simulation, and experimental results are presented, taken from a three-stage laboratory prototype.**

***Index Terms*—Current sharing, dc–dc, dc/dc converters, interleaving, multiphase, paralleled converters, zero-voltage switching (ZVS).**

I. Introduction

TWO OR MORE power stages in a single dc–dc converter can be connected in parallel to increase the output power level. When paralleling dc–dc power converters, each paralleled converter has its own voltage control loop so each can operate either stand-alone or in parallel. Alternatively, for a dc–dc converter containing paralleled power stages, normally, only a single voltage loop is implemented for converter voltage regulation. This paper deals with paralleled power stages. Both parallel dc–dc converters and parallel power stages require current sharing among paralleled power channels. Only then can the design be optimized, ensuring equal temperature rise and minimizing the power rating of the individual components. Paralleled power stages enable the use of standardized designs for different loads; using interleaving techniques can reduce the input and output current and voltage ripples but they are not truly modular because they must share the voltage loop controller.

The simplest concept of paralleling power stages is shown in Fig. 1, where several stages are controlled by a single control loop sharing the same duty cycle. In order to achieve load sharing among the modules, the power stages must be identical in components, board layouts and, particularly, duty ratio [1]–[6]. Since perfect matching is not achievable in practice, this method seems to be unfeasible. Nevertheless, there is a passive balancing mechanism which makes this approach useable, the converter output impedance. High-current power stages

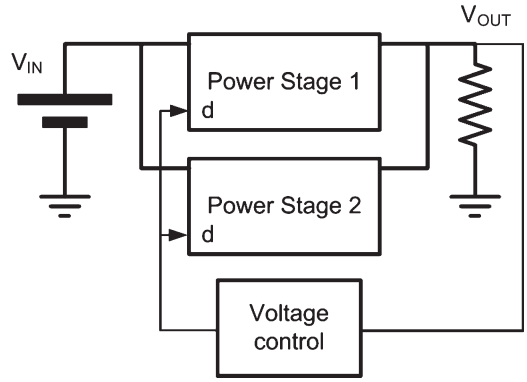

Fig. 1. Concep

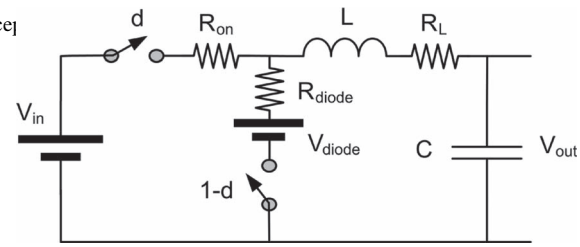

Fig. 2. Paralleled power stage.

usually work in continuous inductor current mode (CCM) with very low output impedance, so the power stage with the highest output voltage will deliver the highest current. During recent years, interleaved buck converters with synchronous rectification have been developed following this simple method [7], [8]. Although these power stages work in CCM, thanks to digital control that ensures very similar duty cycles, the filter inductor resistance and the MOSFET on-resistance are enough to share the currents. In addition, due to the MOSFET resistance positive temperature coefficient, the temperature will have an equalizing effect, increasing the output impedance of the stage with the highest current. However, in topologies with higher output voltages, where free wheeling diodes are used, the temperature effect could completely be different [9].

It is interesting to calculate the necessary output impedance to obtain the desired current share for "*k*" paralleled buck converters as shown in Fig. 2. In the multiphase dc current sharing model shown in Fig. 3, it is assumed that the variation of effective resistance for each phase estimated from (1) can be ignored regarding the added Z_{o}

$$R_{\mathrm{sum}} = d \cdot R_{\mathrm{on}} + (1-d)R_{\mathrm{diode}} + R_{\mathrm{L}} + R_{\mathrm{layout}}. \quad (1)$$

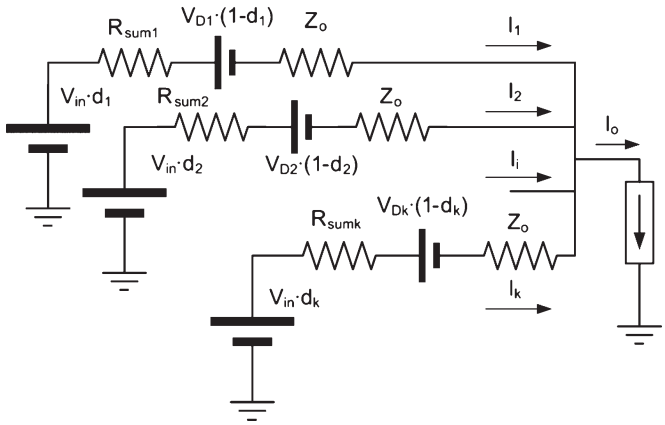

Fig. 3. Multiphase buck converter dc model.

An output voltage mismatch results in the worst case current mismatch, through a particular phase (let it be phase i). This is when phase "i" has the maximum voltage and all other phases have the minimum voltage. The maximum voltage is obtained with the highest duty cycle $(d + \Delta d)$ and the lowest diode voltage drop $(V_{\rm D} - \Delta V_{\rm D})$. Considering second-order terms negligible $(\Delta d \cdot \Delta V_{\rm D})$, current through phase i can be calculated as

$$I_{\rm i} = \frac{V_{\rm in}(d + \Delta d) - (V_{\rm D} - \Delta V_{\rm D})(1 - d) - V_{\rm o}}{Z_{\rm o} + R_{\rm sum}}. \qquad (2)$$

Current trough remaining phases is

$$I_{\rm o} - I_{\rm i} = \frac{V_{\rm in} d - V_{\rm D}(1 - d) - V_{\rm o}}{Z_{\rm o} + R_{\rm sum}}(k - 1). \qquad (3)$$

The mismatch current through phase i can be calculated from (4) as the difference between the current $I_{\rm i}$, (2), and the nominal phase current $I_{\rm o}/k$

$$I_{\rm i} - \frac{I_{\rm o}}{k} = \Delta I_{\rm i} = \left(\frac{k - 1}{k}\right) \frac{V_{\rm in} \cdot \Delta d + \Delta V_{\rm D}(1 - d)}{Z_{\rm o} + R_{\rm sum}}. \qquad (4)$$

According to (4), equalizing resistors can be used to improve the power stage current sharing, although this impedance means high power losses.

Active clamp topologies have been analyzed in different papers from the point of view of zero-voltage switching (ZVS), stability, dynamic behavior, etc. [10]–[16]. In this paper, a new application of the active clamp is proposed: to use the high output impedance of these topologies working as a lossless equalizing resistor.

In [17], it was proved that the active clamp buck converter has high output impedance, but that model did not include clamp capacitor and soft-switching effects in the converter input. In Section II, a complete model is presented, following the method shown in [18]. A multiphase active clamp buck converter design is proposed in Section III, and Section IV provides experimental results for verification. Finally, conclusions are shown in Section V.

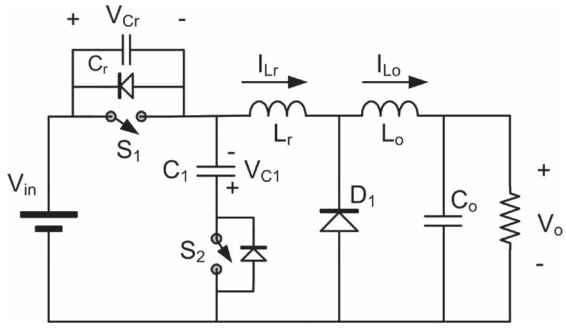

Fig. 4. Active clamp buck converter.

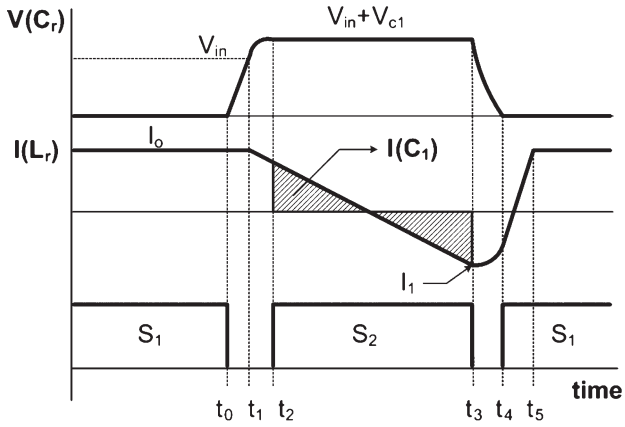

Fig. 5. Converter waveforms.

II. Averaged Switch Modeling

A. Principle of Operation

The active clamp buck converter shown in Fig. 4 has adequately been reported in [19]. Anyway, a simplified analysis will be performed to show the principal voltage and current waveforms (Fig. 5) and the equivalent circuit for the different intervals (Fig. 6). In the steady-state analysis presented here, the filter inductor and the clamp capacitor are assumed to be very large. Therefore, the output current inductor and clamp capacitor voltage are considered constants. The switches S_1 and S_2 are alternately turned on with small dead times to allow soft switching. According to Figs. 5 and 6, the circuit behavior can be divided into six stages

- Stage 1 $(t_0 - t_1)$: Before t_0, S_1 is on, and S_2 is off. At t_0, S_1 is turned off, and $C_{\rm r}$ is linearly charged to $V_{\rm in}$.
- Stage 2 $(t_1 - t_2)$: When $C_{\rm r}$ reaches $V_{\rm in}$, the freewheeling diode D_1 is forward biased. The current through $L_{\rm r}$ and $C_{\rm r}$ evolves in a resonant way and the voltage in $C_{\rm r}$ rises to $V_{\rm in} + V_{C_1}$.
- Stage 3 $(t_2 - t_3)$: As $V_{\rm Cr} = V_{C_1} + V_{\rm in}$, the voltage a cross S_2 is zero, thus S_2 turns on with no losses. The current through $L_{\rm r}$ ramps down. S_2 is turned off at t_3.
- Stage 4 $(t_3 - t_4)$: The voltage a cross $C_{\rm r}$ falls to zero, due to resonance with $L_{\rm r}$.

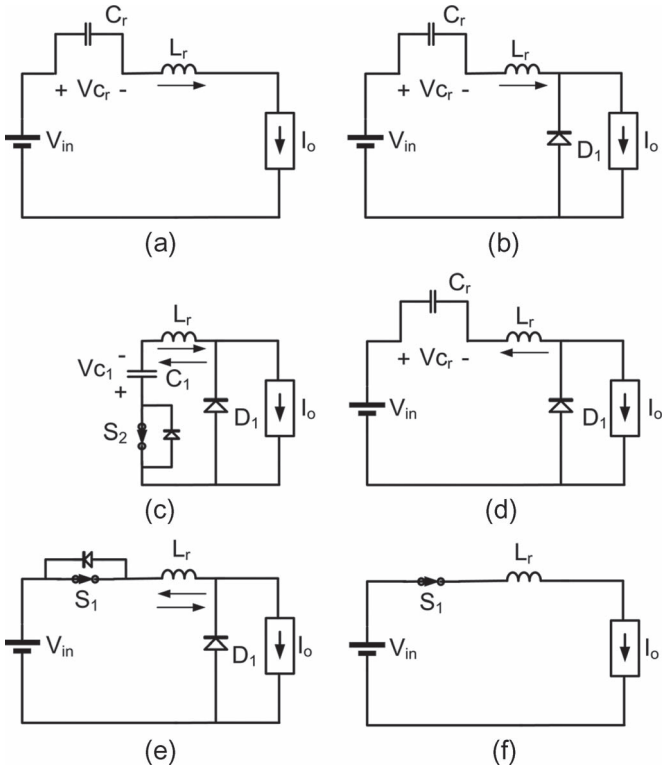

Fig. 6. Stages in a switching period. (a) Stage 1. (b) Stage 2. (c) Stage 3. (d) Stage 4. (e) Stage 5. (f) Stage 6.

Stage 5 $(t_4 - t_5)$: S_1 is turned on with zero voltage and without losses because the voltage at C_r is null. The current through L_r changes the polarity and ramps up until it reaches I_o.

Stage 6 $(t_5 - t_0 + T_\mathrm{s})$: The diode D_1 is reversed biased. At the end of this stage, S_1 is turned off, being the end of a switching period.

B. Averaged Model

According to [18], the resonant transitions, $t_0 - t_2$ and $t_3 - t_4$, are ignored. Therefore, the averaging process must be carried out only for three intervals: t_{3-5} where S_1 and D_1 are on; $d \cdot T_\mathrm{s} - t_{3-5}$ where S_1 is on but D_1 is off; and $(1-d) \cdot T_\mathrm{s}$ where S_1 is off. Where, T_s is the switching period.

The value of the t_{3-5} interval is not controlled by the pulsewidth modulation and is load dependent. Based on I_Lr, the waveform shown in Fig. 5, (5) and (6) can be derived. Hence, t_{3-5} can be expressed as

$$\frac{V_\mathrm{in}}{L_\mathrm{r}} \cdot t_{3-5} = I_0 - I_1 \tag{5}$$

$$\frac{V_{C_1}}{L_\mathrm{r}} \cdot (1-d) \cdot T_\mathrm{s} = I_0 - I_1 \tag{6}$$

$$t_{3-5} = \frac{V_{C_1} \cdot (1-d)}{V_\mathrm{in}} T_\mathrm{s}. \tag{7}$$

It must be noted that in the steady state $I_0 = -I_1$. The clamp capacitor dynamic effect is neglected when I_1 is not included in the analysis.

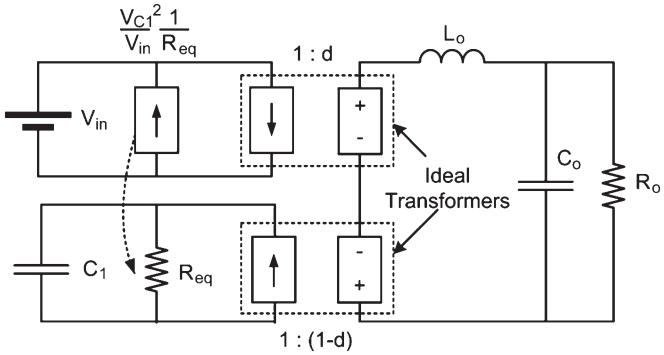

Fig. 7. Active clamp buck converter averaged model.

Equations (8)–(10) have been obtained by averaging the state-space variables I_Lo, V_o, and V_{C_1} for the three time intervals presented above

$$\overline{i_{C_\mathrm{o}}} = C_\mathrm{o} \frac{d\overline{v_\mathrm{o}}}{dt} = \overline{i_{L_\mathrm{o}}} - \frac{\overline{v_\mathrm{o}}}{R} \tag{8}$$

$$\overline{v_{L_\mathrm{o}}} = L_\mathrm{o} \frac{d\overline{i_{L_\mathrm{o}}}}{dt} = \overline{v_\mathrm{in}} d - \overline{v_{C_1}}(1-d) - \overline{v_\mathrm{o}} \tag{9}$$

$$\overline{i_{C_1}} = C_1 \frac{d\overline{v_{C_1}}}{dt} = \overline{i_{L_\mathrm{o}}}(1-d) - \frac{\overline{v_{C_1}}}{2L_\mathrm{r} f_\mathrm{s}}(1-d)^2. \tag{10}$$

To complete the averaged circuit, it is necessary to include the averaged input current that is defined by (11) and (12), where f_s is the switching frequency

$$\overline{i_\mathrm{in}} = \overline{i_{L_\mathrm{o}}} d - \frac{V_{C_1}^2}{V_\mathrm{in}} \frac{1}{R_\mathrm{eq}} \tag{11}$$

$$R_\mathrm{eq} = \frac{2L_\mathrm{r} f_\mathrm{s}}{(1-d)^2}. \tag{12}$$

The averaged equivalent circuit that can be derived from (8)–(12) is shown in Fig. 7. However, to obtain a more accurate model, an output filter inductor equivalent resistance and output filter capacitor equivalent resistance can be added.

C. Small Signal Model

The averaged model obtained in the previous section is clearly nonlinear. After linearization of (8)–(10), defining the steady-state equilibrium as (D, V_in, V_o, V_{C_1}, I_Lo), the system state-space representation, where u is the vector of inputs, y is the system output, and x is the state variables vector, is

$$\dot{x} = Ax + Bu \tag{13}$$

$$y = Fx + Gu \tag{14}$$

where $x = [i_\mathrm{Lo}\ v_{C_1}\ v_\mathrm{o}]^\mathrm{T}$, $u = [v_\mathrm{in}\ d]^\mathrm{T}$, $y = v_\mathrm{o}$, $F = [0\ 0\ 1]$, $G = [0]$, and

$$A = \begin{bmatrix} 0 & \frac{-(1-D)}{L_\mathrm{o}} & -\frac{1}{L_\mathrm{o}} \\ \frac{1-D}{C_1} & -\frac{1}{R_\mathrm{eq} C_1} & 0 \\ \frac{1}{C_\mathrm{o}} & 0 & \frac{-1}{RC_\mathrm{o}} \end{bmatrix}$$

$$B = \begin{bmatrix} \frac{D}{L_\mathrm{o}} & \frac{V_\mathrm{in}+V_{C_1}}{L_0} \\ 0 & \frac{V_{C_1}}{L_\mathrm{r} f_\mathrm{s} C_1}(1-D) - \frac{I_{L_\mathrm{o}}}{C_1} \\ 0 & 0 \end{bmatrix}.$$

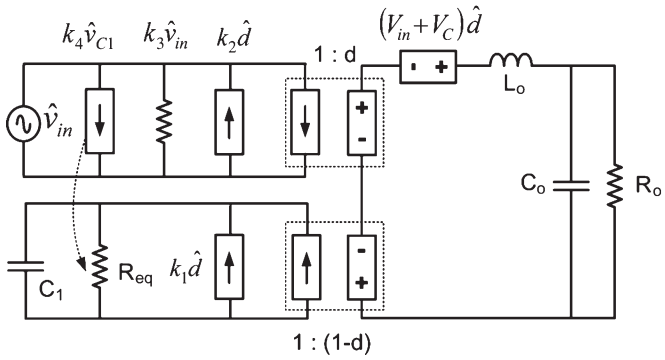

Fig. 8. Small-signal model. Constants k_1, k_2, k_3, and k_4 can be found in Table I.

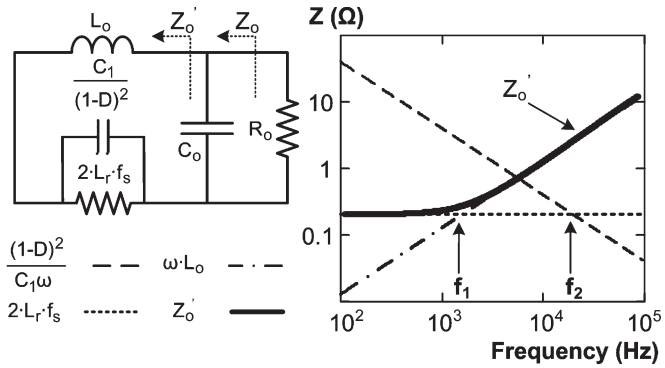

Fig. 9. Equivalent circuit to obtain output impedance $Z_{\rm o}$.

TABLE I
CONVERTER SMALL SIGNAL MODEL PARAMETERS

Parameter	Value
k1	$\frac{V_{C_1}}{L_r f_s}(1-D)-I_{L_o}$
k2	$I_{L_o}+\frac{2V_{C_1}^2}{V_{in}}\frac{1}{2L_r f_s}(1-D)$
k3	$-\frac{V_{C_1}^2}{V_{in}}\frac{1}{R_{eq}}$
k4	$2\frac{V_{C_1}}{V_{in}}\frac{1}{R_{eq}}$

The small-signal equivalent circuit derived from the above equations is represented in Fig. 8. It must be noted that in Section I, the output impedance was presented as a method for current sharing in multistage converters. Now, the output impedance can be calculated from the circuit in Fig. 9. This circuit is obtained from the small-signal model where $\hat{d} = \hat{v}_{\rm in} = 0$.

The dc output impedance represented by (15) is the defined equivalent resistor $R_{\rm eq}$ seen from the ideal transformer secondary side. Therefore, the dc output voltage can be expressed as

$$Z_{\rm o(dc)} = 2L_{\rm r}f_{\rm s} = R_{\rm eq}(1-D)^2 \quad (15)$$

$$V_{\rm o(dc)} = V_{\rm in}D - 2L_{\rm r}f_{\rm s}I_{\rm o}. \quad (16)$$

TABLE II
CONVERTER OPERATING VALUES IN SIMULATION

Parameter	Value	Parameter	Value
$\mathbf{V_{in}}$	120 V	$\mathbf{C_o}$	4 µF
$\mathbf{V_o}$	48 V	$\mathbf{L_o}$	86.4 µH
D	0.5	$\mathbf{C_r}$	2 nF
$\mathbf{f_s}$	100 kHz	$\mathbf{L_r}$	6 µH
P	480 W	$\mathbf{C_1}$	2 µF
R	4.8 Ω		

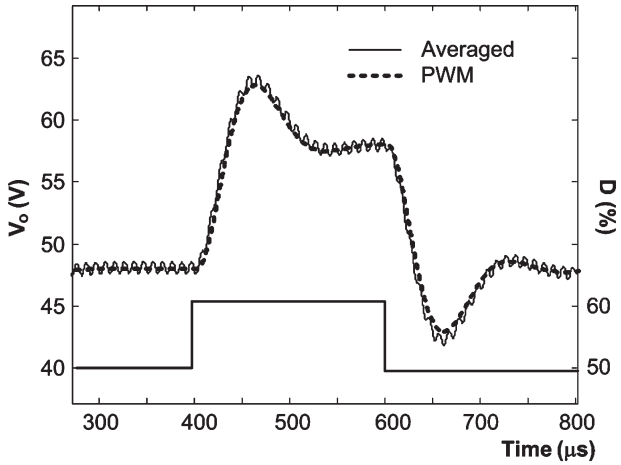

Fig. 10. Converter output voltage and average model voltage.

As the three converters have the output connected in parallel, the output capacitor $C_{\rm o}$ does not affect the current sharing. Therefore, the impedance that carries out the current distribution is $Z_{\rm o}'$, Fig. 9. Whenever the frequency f_2 is higher than f_1, as it happens most of the times, the smallest impedance that will process the current sharing will be $Z_{\rm o(dc)}$. In that way, assuming that $f_1 < f_2$, $Z_{\rm o(dc)}$ is responsible for current distribution in the worst case. Also, if, due to tolerances, there are differences in $C_{\rm r}$, C_1, or $L_{\rm r}$, it will not affect the current sharing.

D. Averaged Model Validation

A simulation has been performed to estimate how accurately the model matches the converter. The converter parameters can be found in Table II.

The converter dynamic response to a duty cycle step is represented in Figs. 10 and 11, where it can be noted that currents and voltages in the average model are in good agreement with currents and voltages in the simulated switch converter.

However, the model is not always correct. The result has been obtained by assuming that the period of time while S_1 is on is exactly controlled by its gate control signal. To ensure the existence of ZVS a dead time must be introduced [15], [16], [19]. S_1, the internal diode is on immediately after S_2 is turned off. Therefore, the effective on period starts when S_2 is turned off and finishes when S_1 is turned off. This "effective duty cycle" is bigger than that used in the model. Therefore,

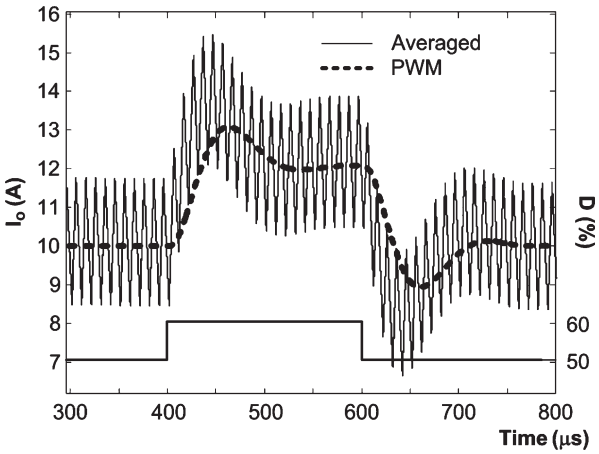

Fig. 11. Output filter inductor current and average model current.

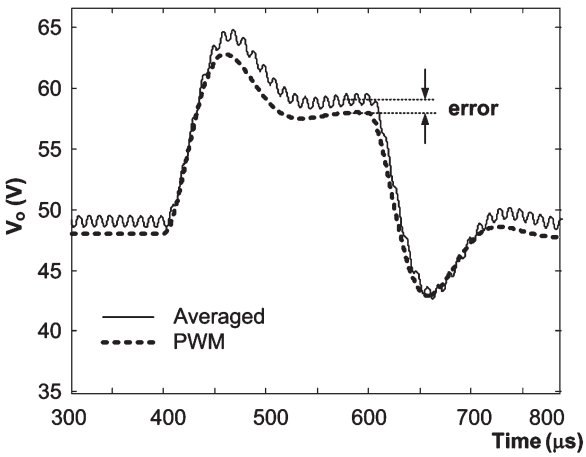

Fig. 12. Error between the converter and averaged model, when dead time is not negligible.

as shown in Fig. 12, when the dead time is not negligible with respect to the "on" control signal, the duty cycle error can be appreciable using this model.

III. Multiphase Active Clamp Buck Converter

In Section I, (4) was derived to calculate the equalizing resistor. This resistor ensures, in the worst case, that current mismatch will not exceed the design limits. In Section II, the converter output impedance was given by (15). Now, using (4) and (15) together with the design conditions, the value of $L_{\rm r} \cdot f_{\rm s}$ can be calculated. For example, a three-stage buck converter without an equalizing resistor and with design conditions: $d = 0.5$, $\Delta d = 0.01$, $R_{\rm sum} = 0.05\ \Omega$, $V_{\rm in} = 30$ V, and $\Delta V_{\rm DIODE} = 0.2$ V would have a current unbalance of 5.33 A. Using a 0.216 Ω equalizing resistor, the maximum current variation would be 1 A. The switching frequency has probably been selected before the equalizing resistor calculation so the resonant inductance $L_{\rm r}$ can easily be calculated. Nevertheless, to ensure the ZVS operation, the energy stored in $L_{\rm r}$ when S_2 is turned off must be greater than the energy required to discharge $C_{\rm r}$ from $(V_{\rm in} + V_{C_1})$ to 0. Considering that the output filter current ripple could be neglected, the ZVS condition can be expressed as (17). Here, the steady-state clamp capacitor voltage expressed in (18) can be derived from (6) assuming that $I_{\rm o} = -I_1$

$$\frac{1}{2} L_{\rm r} I_{\rm o}^2 \geq \frac{1}{2} C_r (V_{\rm in} + V_{C_1})^2 \tag{17}$$

$$V_{C_1} = \frac{Z_{\rm o\_dc} \cdot I_{\rm o}}{(1-D)} = \frac{Z_{\rm o\_dc} \cdot I_{\rm o} \cdot V_{\rm in}}{V_{\rm in} - V_{\rm o} - Z_{\rm o\_dc} \cdot I_{\rm o}}. \tag{18}$$

For the same output impedance, a higher frequency means a lower resonant inductor but increases the minimum load value to ensure soft-switching transitions. In order to ensure ZVS operation for low loads, an output impedance higher than the obtained with (4) can be used. However, it must be taken into account that very high output impedance can penalize the converter global efficiency due to the processed extra energy that is returned to the input source.

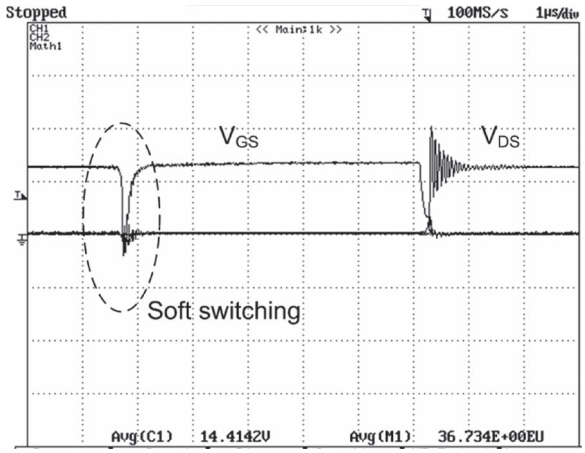

Fig. 13. S_1 ZVS operation, Load = 5 A. Transistor drain-to-source voltage is null before the transistor is turned on.

IV. Experimental Results

To test the current sharing due to the high output impedance, a three-phase ZVS active clamp buck converter was implemented. The converter was designed with the following parameters: $V_{\rm in} = 30$ V, $V_{\rm o} = 13$ V, $\rm P_o = 3 \times 100$ W, $f_{\rm s} = 100$ kHz, $d = 0.5$, $L_{\rm o} = 20\ \mu$H, $L_{\rm r} = 1\ \mu$H, $C_{\rm r} = 2.2$ nF, $C_{\rm o} = 390\ \mu$F, $\rm ESR_{Co} = 0.068\ \Omega$, and $C_1 = 10\ \mu$H. IRF540 and MBR1045 are used as switching devices and rectifier diode, respectively. Resonant inductances were coil-craft SER2010 (1 μH) with measured values: $L_{\rm r1} = 1.067\ \mu$H, $L_{\rm r2} = 1.033\ \mu$H, and $L_{\rm r3} = 1.068\ \mu$H. Every stage has small differences with respect to the others including different heat sinks, layouts, and component tolerances. Differences among the resonant inductors will lead to differences of output impedance and current distribution. Also, differences among the output inductors will lead to differences in the current ripple. The nominal output inductor is 20 μH, but due to tolerances, the output inductor for each phase is as follows: $L_{\rm o1} = 22.47\ \mu$H, $L_{\rm o2} = 25.97\ \mu$H, and $L_{\rm o3} = 22.5\ \mu$H.

The dc output impedance (Table III), ZVS operation (Fig. 13), and efficiency (Fig. 14) have been measured for each stage.

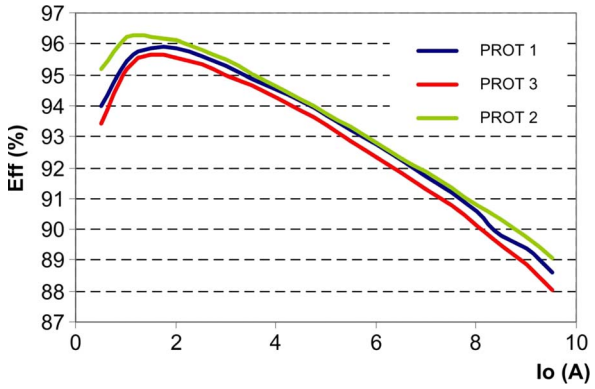

Fig. 14. Prototype efficiency.

TABLE III
MEASURED AND CALCULATED OUTPUT IMPEDANCE

Phase	Theoretical	Measured
1	0.27 Ω	0.32 Ω
2	0.25 Ω	0.30 Ω
3	0.31 Ω	0.33 Ω

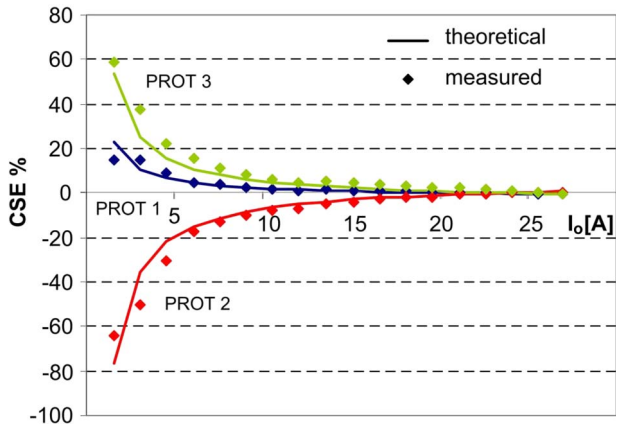

Fig. 15. Theoretical and measured current distribution for different loads.

The output impedance must also take into account the transistor static drain to source on resistance, the diode forward slope resistance, and the output filter inductor resistance. Table III shows the expected and measured output impedance for each phase.

From the measured output impedance, the current distribution between phases can be estimated. This has been defined as the relative current sharing error (CSE) for a module and is the current deviation from the expected one for each phase (19). As shown in Fig. 15, the measured and calculated CSE for different loads are in good agreement

$$\text{CSE}\% = \frac{I_\text{i} - I_\text{o}/3}{I_\text{o}/3} 100. \tag{19}$$

To test the interleaving behavior a "Digilab 2" development board for the Spartan II was used to generate the phase shifted driver signals, as shown in Fig. 16. The interleaved output inductor currents can be seen in Fig. 17. Small differences can be seen among currents due to tolerances in the resonant

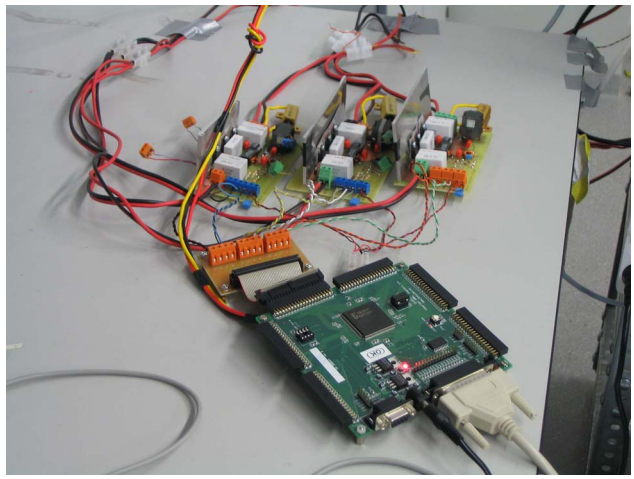

Fig. 16. Interleaved active clamp buck converter prototype.

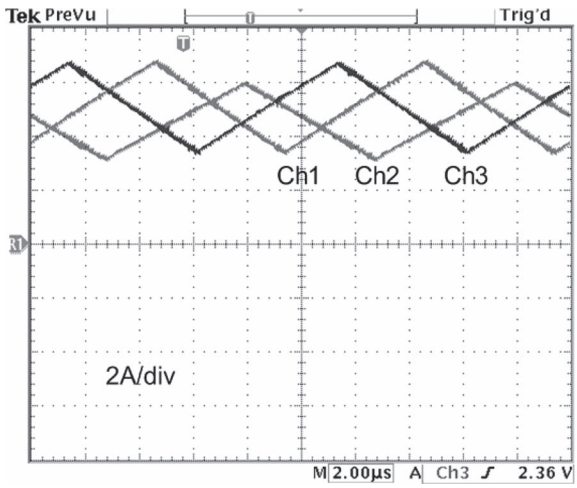

Fig. 17. Interleaved output inductor currents. Load = 15 A. 2 A/div.

inductors. Differences among the output inductors will give rise to differences in the output filter current ripple. Nevertheless, the current mismatch is small for a three nonidentical stage converter.

Fig. 18 shows the current distribution for the three-phase converter, where one phase has a mismatch in duty cycle. Now, two phases, prototypes 1 and 3, have a duty cycle of 50%, and the third one has a 51%. Due to the increment, when the total output current is 18.6 A, from (4), the currents must be $I_1 = 5.86$ A, $I_3 = 5.86$ A, and $I_2 = 6.86$ A, as shown in Fig. 18. Deviation in voltage diode ΔV_D has not been included.

In Section II, the average model has been validated with simulations. For phase 1, control-to-output transfer function and the output impedance have been measured with the HP4395 network analyzer. As shown in Figs. 19 and 20, the model predictions match well the measured results. The probe gain and bandwidth together with power supply output impedance are included in simulations and measurements.

V. CONCLUSION

The output impedance of the active clamp buck converter has been modeled including the clamp capacitor effect. This

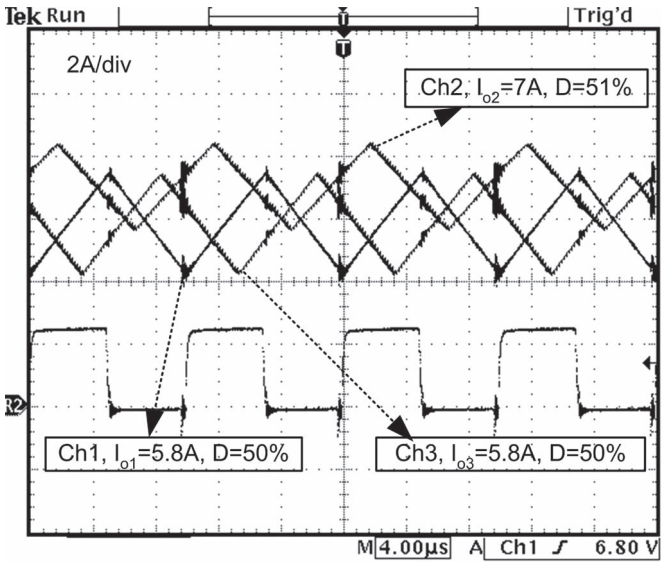

Fig. 18. Interleaved output inductor currents. Load = 18.6 A, 2 A/div.

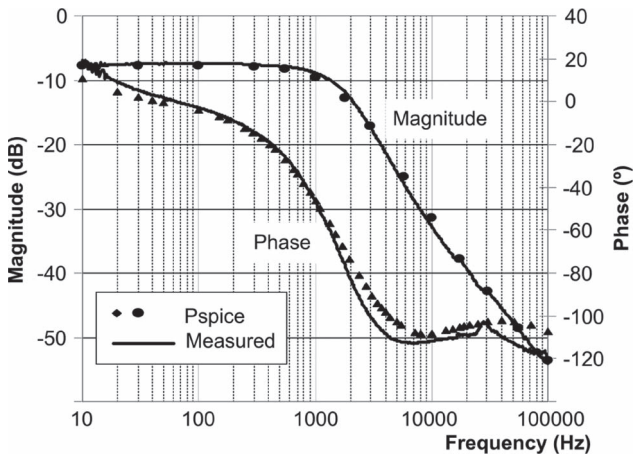

Fig. 19. Simulated and measured control-to-output Bode diagram. Probe gains are included.

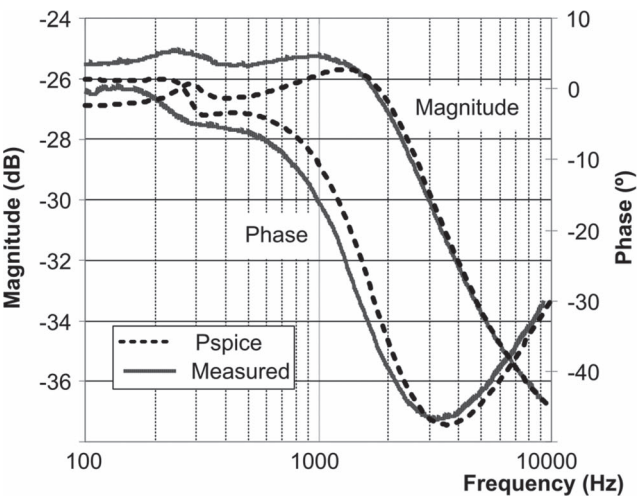

Fig. 20. Simulated and measured output impedance Bode diagram. Probe gains and power supply output impedance are included.

output impedance has been proposed and tested as a method to equalize currents among k parallel stages. This method does not require any current sensor or control loop and can be designed to avoid current imbalances even in the presence of large duty cycle mismatches. Experimental results have been obtained with three different prototypes connected in parallel but current sharing has not been affected. Anyway, differences among the resonant inductors will take to differences among output impedances and, therefore, to current distribution. However, it is easier to pay attention only to this parameter instead of the full converter.

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