Low Power 9-bit 500 kS/s 2-Stage Cyclic ADC using OTA Variable Bias Current

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Abstract

This paper presents a 9-bit, 2-stage cyclic analog to digital converter (ADC) with a variable bias current control circuitry to reduce its power dissipation. Each stage outputs a three-bit digital word and the circuit requires four subcycles to perform a whole conversion. Since the accuracy required is higher in the first stage and first subcycle and decreases in subsequent cycles, the bias current of each operational transconductance amplifier (OTA) is regulated depending on the subcycle of the conversion process. The resolution and sampling frequency of the converter make it suitable to be integrated with 8-bit CMOS imagers with column-parallel ADC architectures. The ADC has been designed using a 1.2 V 110 nm CMOS technology and the circuit consumes 27.9 µW at a sampling rate of 500 kS/s. At this sampling rate and at a 32 kHz input frequency, the circuit achieves 56 dB of SNDR and 9 bit ENOB. The Figure of Merit is 109 fJ/step.

Keywords: Analog-to-digital converter (ADC); CMOS; OTA; low power; adaptive bias current.

1. Introduction

Analog to digital converters are circuits required in most CMOS image sensors built nowadays. These circuits usually require low power ADCs, with a resolution above 8 effective bits, very little noise and a frame rate above 30 frames per second or faster. Typical ADCs topologies employed in CMOS imagers are successive approximation (SAR) and cyclic converters [1]. Most CMOS imagers use column parallel ADC architectures, which implies that there are as many ADCs as columns in the imager, and each ADC must convert the values of the pixels of the whole column. This leads to two types of design considerations. On the one hand, the design of ADC architectures with moderate speeds and medium resolution. In the case of CMOS image sensors using 256 gray level, at least 9-bit

resolution ADCs are needed, usually having a measured effective number of bits (ENOB) of between 8 and 9 bits. On the other hand, each converter must fit within the width of an imager column, which implies some area restrictions. Although SAR converters are simple and efficient, they tend to occupy a larger area since its DAC requires 2^n capacitors, being n the resolution of the converter, compared to only two capacitors per stage required by a cyclic circuit [2]. Moreover, their performance can be limited by the comparator input noise and by the output amplifier because of the lack of a residue amplification circuit, which is included in the cyclic converter. In fact, other requirements of the comparator such as power consumption, offset error and response time can be a serious handicap to reach the global specifications of the ADC. Alternatively, pipelined cyclic ADC can be presented as a possible converter for these type of applications. Despite their performance being limited by capacitor matching, both capacitors mismatch and comparator offset can be corrected in the digital domain because of the redundant bits generated by each stage. This allows the strong relaxation of the requirements of the comparator. Thus, the design challenge is to cut down on cyclic converters power dissipation while keeping their performance.

The literature shows different cyclic converters which accomplish the aforementioned specification. In [3] a 50 MS/s 9-bit ADC consuming 6.9 mW is presented. Also, in [4] and [5], 9-bit designs with sampling frequencies in the range of MS/s and power dissipations in the range of miliwatts are proposed. Lower power circuits are described in [6] and in [7] where a 10 kS/s 9-bit resolution cyclic ADC consuming 11µW is proposed. Power dissipation is a key specification when designing ADCs, as the current growing market of portable electronic devices demands low power consumption circuits. Regarding cyclic and pipelined ADCs, which are based on the same principles as cyclic ones, different techniques to reduce the power dissipation can be found in the literature. Given that operational amplifiers are the circuits with higher power dissipation inside an ADC, a first approach consists of reducing the power dissipation of these elements. This reduction is usually done using stage scaling techniques [8], where the switched capacitor circuits in each stage are determined by noise requirements. It is well known that the thermal noise contribution of a given stage is reduced by the gain of the previous stage. This allows a scaling down of the capacitor in that stage. Other approaches employ current-reuse methods which reuse the bias current for the current-steering DAC and the linear OTA [9] and provide an overall bias current reduction. This architecture is employed however to compensate residue gain and nonlinearity errors. Another common technique consists of powering off OTAs in the sampling phase [10-14], which provides appreciable power savings. This approach is possible because in pipeline ADCs, the stages work alternatively in sampling and amplification phases. However, there are design challenges related to the fast OTA turn-on time. A further step is based on sharing the same amplifier between two adjacent ADC stages [15] [16]. This technique, which implies a reduction of up to half the number of amplifiers, theoretically also reduces the whole circuit power dissipation by about one half. A third technique takes advantage of the fact that the bias current required

by amplifiers depends on the stage in which they are working. So, a circuit varying the bias current of an amplifier, depending on the stage, contributes to cut down on power dissipation. An example of this technique applied to a 5-stage pipeline ADC is described in [17]. Finally, in [18] a reconfigurable pipeline converter employing parallel OTAs to reach optimal power dissipation over a wide sampling rate range is proposed. However, this technique requires to increase the number of OTAs in each stage, which in turns leads to increase the complexity and the size of the circuit.

In this paper, a technique to regulate the amplifiers bias current in a 9-bit cyclic ADC is presented. In order to exploit this power reduction technique, the converter is based on a two-stage architecture which allows to balance the advantages of pipelined and pure single-stage cyclic circuits. The ADC has been designed for a sampling frequency of 500 kS/s, to be used in CMOS image sensors having column parallel ADC architectures. As previously mentioned, in a pipeline ADC, the thermal noise contribution of a given stage is reduced by the gain of the previous stage. In the case of a cyclic ADC, this means that noise requirements are reduced in subsequent cycles of operation. Thus, the bias current will depend on whether a) the stage is sampling or amplifying or b) for a given input sample, on which cycle, first or second, the ADC is working. The rest of the paper is organized as follows: section II describes the architecture of the proposed converter and the architecture of the OTAs using adaptive bias current. Results obtained from device level simulations are shown in Section III. Finally, conclusions are drawn in Section IV.

2. Circuit Implementation

Figure 1 shows the structure of the cyclic ADC that is proposed in this work. The circuit is composed by two stages working in opposite clock phases with a conversion schema of 2.5 bit per stage, and a Redundant-Signed-Digit architecture (RSD) to obtain a 9 bit output. In each stage, the input signal is quantized by a 3-bit flash ADC and then digitized again through a digital to analog converter (DAC). The difference between this last signal and the input signal is called residue. The residue is then amplified and passed on to the next stage, where the same process is repeated. The DAC, the Sample & Hold (S/H) and the amplifier make up the Multiplying Analog to Digital Converter (MDAC). The converter has been synthesized using a fully differential configuration to improve the immunity to common-mode non-desired signals, although in the figure it has been represented as a single ended circuit for simplification purposes.

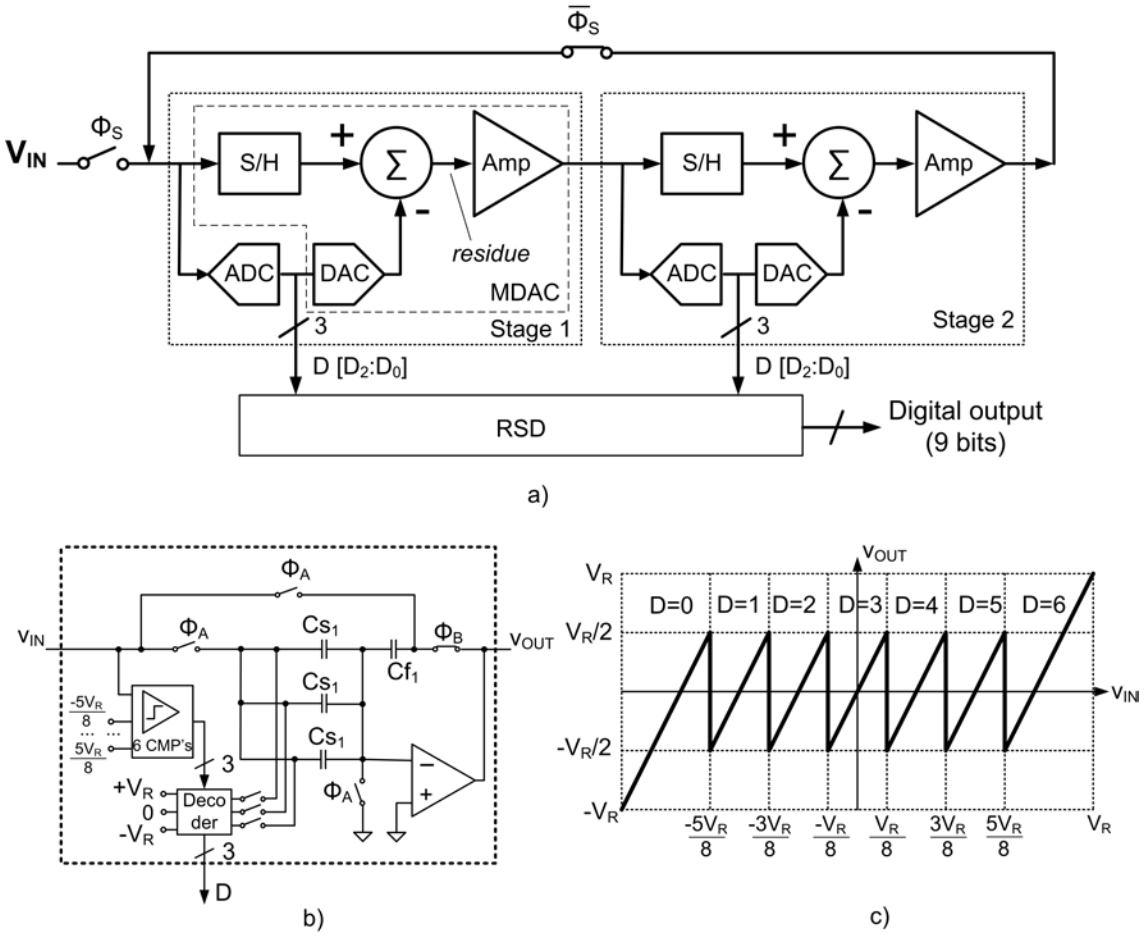

Fig. 1 2-stage cyclic ADC. a) Circuit structure b) Stage architecture c) Transfer function.

Figure 1.b shows the internal structure of the first stage. The 3-bit flash ADC is made up of six comparators and generates a seven-state digital code D = [D2:D0], having a value ranging from zero to six. This code constitutes the stage digital output and also drives the decoder selecting the reference voltage for each capacitor Cs. The output voltage is given by the following equation:

$$Vout = \left(1 + \frac{\sum Cs}{Cf}\right) \cdot Vin + \frac{\sum Cs}{Cf} \cdot V_R \qquad (1)$$

where V_R is the reference voltage level. For Cs=3·Cf, the gain is four and the value of the offset term is determined by the flash ADC, according to:

$$\frac{\sum Cs}{Cf} \cdot V_R = \begin{cases} 3V_R & if\ D = 0; \quad -V_R \quad if\ D = 4 \\ 2V_R & if\ D = 1; \quad -2V_R \quad if\ D = 5 \\ V_R & if\ D = 2; \quad -3V_R \quad if\ D = 6 \\ 0 & if\ D = 3; \end{cases} \qquad (2)$$

The ideal transfer function of this stage is given by (1) and (2) and is shown in Fig 1.c

The structure of the second stage is similar to the first one except that the clocks work in opposite phase and the capacitors are scaled down as the accuracy requirements for this second stage are not as

restrictive as those of the first stage. As shown in Fig. 2, the circuit requires four subcycles to complete the digital conversion of an input sample. Its operation is the following. During the first subcycle, the input voltage is sampled in stage 1. In this subcycle, ϕ_S, and ϕ_A are high and ϕ_B is low, and V_{IN} is sampled by capacitors Cs and Cf. In the next subcycle, the bottom plate of capacitors Cs are connected to V_R, 0 or $-V_R$ to obtain a value of offset voltage according to (2). The residue value is then amplified by stage 1 and, simultaneously, sampled by stage 2. In the third subcycle the residue of stage 2 is amplified and cycled back to stage 1, where it is sampled. Finally, in the fourth subcycle, the amplified residue of stage 1 is sampled again by stage 2. In each subcycle, the circuit outputs a three-bit digital word according to the following sequence of subcycles 2→3→4→1. In the figure, D_1 and D_2 represent the codes created by stages 1 and 2 respectively. Thus, after four subcycles a 12-bit digital word is obtained. This word is then processed by the RSD algorithm to finally give rise to the 9-bit digital word.

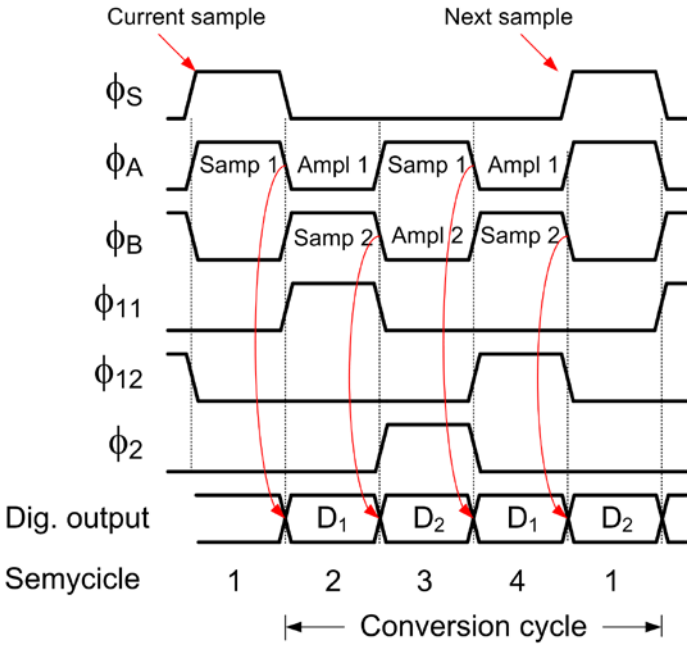

Fig. 2 Control signals of the ADC and the OTAs.

Figure 3 shows the structure of the amplifier used in the first stage of the amplifier (OTA1). This is a fully differential symmetrical OTA with gain boosting, where A1 and A2 are the boosting amplifiers. In a cyclic ADC, both the working cycle and the stage define the main requirements regarding performance parameters, such as settling time, resolution, closed-loop gain, bandwidth, slew rate, etc. Therefore, the slew rate of OTAs will be higher in the first working cycles since the accuracy requirements are more restrictive. This means that the same stage in different working cycles will have different requirements in power consumption if an efficient design were to be implemented.

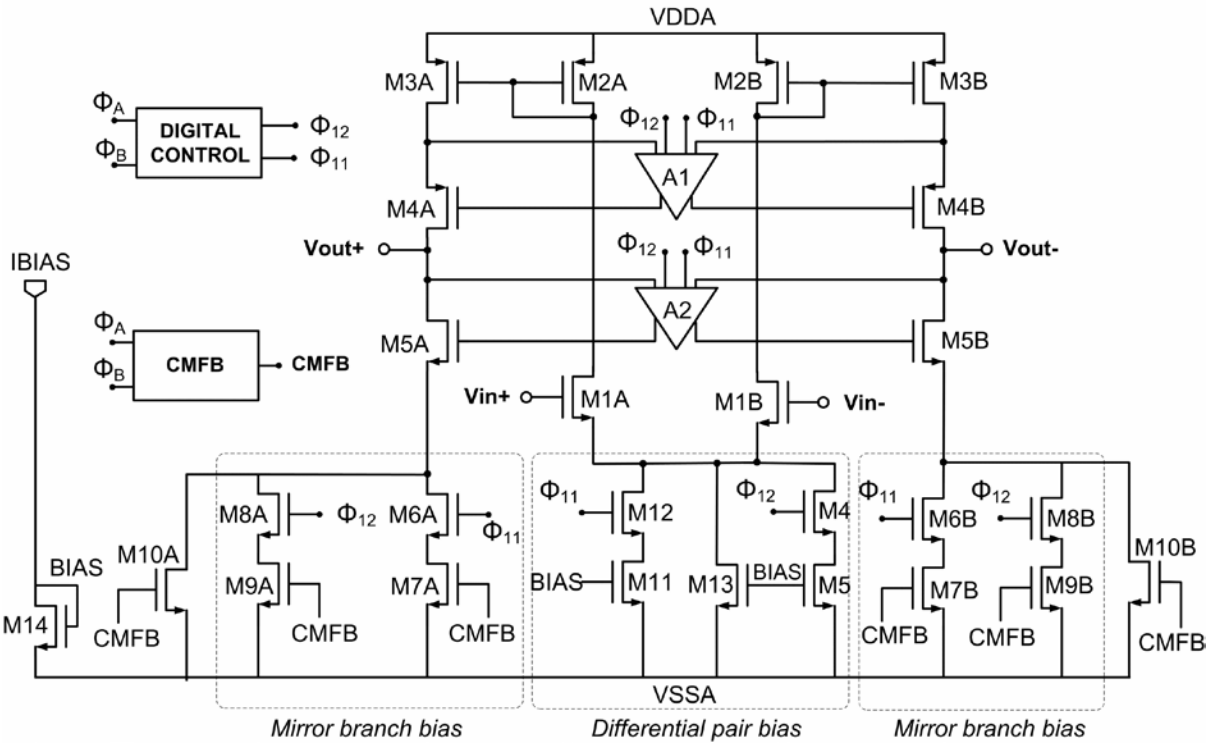

Fig. 3 Structure of the OTA used in the first stage.

The total setting time of the amplifier (T_{Total}) can be divided into large signal settling time (T_{LS}) and small signal setting time (T_{SS}). Large signal settling time is defined mainly by the slew rate. In a symmetrical OTA, the maximum slew rate is defined as follows:

$$Slew\ Rate = \frac{I_{OUT}}{C_L} = \frac{V_{FS}}{T_{LS}} \qquad (3)$$

where I_{OUT} is the output current, C_L is the load capacitance of the OTA and V_{FS} is the output voltage dynamic range. Taking into account that the maximum output current that can be reached corresponds to the bias current through the mirror branches and that C_L is internally fixed, the OTA needs to regulate its mirror branches bias current dynamically to obtain an efficient design in each working cycle. The main challenge of this design consists of adapting the bias current to the working cycle in a fast way while meeting the requirements of each stage, such as common mode voltage regulation and linearity for each working cycle. The circuit comprises three biasing sub-circuits, one to bias the input differential pair, and two to bias the respective mirror branches. In each biasing subcircuit two control signals, ϕ_{11} and ϕ_{12}, drive respective parallel connected biasing devices; i.e. ϕ_{11} drives devices M6 and M12 and ϕ_{12} drives devices M4 and M8. This structure allows regulating the biasing current depending on the subcycle in which the ADC is working. This OTA only works during subcycles 2 and 4, when the stage 1 is amplifying the residue voltage. During subcycle 2, signal ϕ_{11} is ON (Fig. 2), and the three biasing circuits are driving the maximum current (through devices M6-M7

and M11-M12). However, the biasing current required during subcycle 4 is lower than that needed during subcycle 2, since the required accuracy is also lower. Thus, in this subcycle, signal ϕ_{12} is ON. To avoid a malfunctioning of common mode voltage circuits, the input differential pair is always biased to a minimum current value by device M13. Similarly, devices M10 provide a minimum bias current to the mirror branches. This allows keeping the common mode voltages of the two OTAs at an adequate value throughout the conversion process. This state of minimum bias current is activated during subcycles 1 and 3, where this OTA is not amplifying. The adaptive bias current technique was also applied to the gain boosting of the OTA. The bias current of the gain boosting amplifiers A1 and A2 is also regulated through control signals ϕ_{11} and ϕ_{12} to ensure a robust synchronization.

A similar structure is used in the OTA biasing circuit at its second stage (OTA2), as it is shown in Fig. 4. However, given that the noise requirements of both stages are different, this OTA is slightly different from that used in the first stage. The biasing circuitry is, however simplified when compared to that used in OTA1, since stage 2 only performs one amplification during the conversion cycle. Thus, a single control signal ϕ_2 is used. In this case, devices M8 and M9 provide a minimum bias and output current, while devices M6 and M10 driven by signal ϕ_2 provide extra current. Moreover, similarly to the OTA of the first stage, devices M8 and M11 provide a minimum bias current to the mirror branches and to the input differential pair, respectively. As per the regulation of the bias current of the gain boosting amplifiers A1 and A2 of OTA2, regulation is achieved through control signal ϕ_2

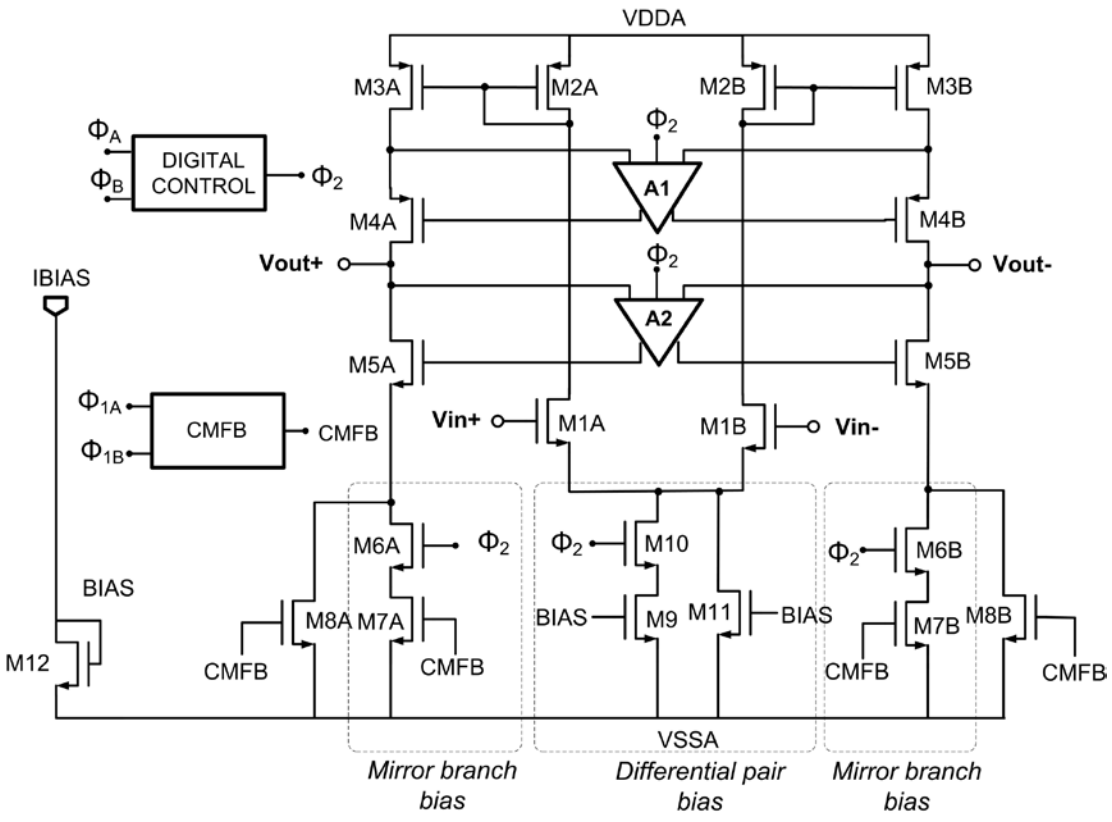

Fig. 4 Structure of the OTA used in the second stage.

As a result, the bias current of the whole ADC reaches its maximum value during subcycle 2 and is progressively reduced to the minimum value in the rest of the subcycles. In the first subcycle, no amplification is performed. Thus, signals ϕ_{11} and ϕ_{12} of OTA 1 are low, as so is signal ϕ_2 of OTA 2. According to the previously described operation of the ADC, stage 1 amplifies during subcycles 2 and 4, while stage 2 amplifies during subcycle 3. The bias current required reaches its peak in the second subcycle and then decreases progressively in subcycles 3 and 4. Thus, from a power consumption perspective, stage 1 has three states of operation (cycles 1 and 3, cycle 2 and cycle 4) and stage 2 has two states of operation (cycles 1,2 and 4 and cycle 3).

3. Simulation Results

The ADC has been synthesized in a 110 nm CMOS process from LFoundry. Power consumption of the analog part of the converter is 27.9 µW at a supply voltage of 1.2 V and a sampling rate of 500 kS/s. The values of the capacitors are C_{f1}=21.1fF, $C_{s1}=3\cdot C_{f1}$, C_{f2} = 9.54 fF, $Cs_2=3\cdot C_{f2}$. In this ADC, the design specifications of the OTAs were previously stablished with the aim of reducing power consumption. The relationship between T_{LS} and T_{Total} was chosen based on previous experience in the design of ADCs and the requirements of each stage and working cycle. Therefore, the general design condition for the design was:

$$T_{LS} \approx 0.1 \cdot T_{Total}. \quad (5)$$

On the other hand, $V_{FS,stage\_cycle}$ is defined by the resolution required in each subcycle and stage:

$$V_{FS,stage\_cycle} = V_{FS} - \frac{V_{FS}}{V_{FS}^{N_{stage\_cycle}}} \quad (6)$$

where $N_{stage\ and\ cycle}$ is the minimum resolution required in each stage and working subcycle. Table 1 shows the values of the biasing current required for each OTA depending on the subcycle in which they are working. For a sampling frequency of 500 kS/s, the maximum settling time is T_{Total} = 500 ns, and according to (4), T_{LS} = 50 ns. The values of the *Slew Rate* are obtained by combining (3) and (5). Finally, parametric simulations were performed to tune the mirror branch bias currents required to achieve the slew rates shown in the table.

Table 1. Slew rate and bias current for each OTA and working subcycle.

Subcycle	OTA	T_{LS} (ns)	N_{stage_cycle}	Slew Rate (MV/s)	Mirror branch Bias current (µA)
2	1	50	10	11.99	2.95
3	2	50	7	11.9	2.27
4	1	50	4	1.12	1.55

Table 2 shows the variation of performance of OTA 1 and OTA 2 depending on the cycle in which they are operating. Since the requirements in each subsequent subcycle of operation are not as restrictive, OTAs performance also decreases in the respective subcycles.

Table 2. OTA AC performance in each subcycle.

Parameter	OTA 1 (subcycle 2)	OTA 2 (subcycle 3)	OTA 1 (subcycle 4)
Power Supply (V)	1.2		
DC Gain	75.19 dB	72.76 dB	70.29 dB
Unity Gain Freq (MHz)	71.95	62.82	39.19
Phase Margin (deg)	56.15	62.82	60.18
Load Capacitance (fF)	200		
Input DC voltage (V)	0.6		
Output Swing (Vpp)	1.2		

Figure 5 shows the AC simulations in open loop for each OTA and cycle. The strictest requirements are set for OTA 1 during the second subcycle. In this case, it is necessary to achieve a DC gain higher than 60 dB. These AC simulations show that, for OTA 1, during the second subcycle, the DC gain is close to 75 dB. The rest of the cases, also show similar values in DC gain, thus the AC requirements are widely met.

Fig. 5 AC response of the OTA1 for the cycles 2 and 4 and OTA2 for the cycle 3.

Figure 6 shows the result of a transient simulation. This figure shows the ADC and S&H input voltages evolution, the output voltage of each OTA, the bias current in each OTAs, and the ADC current consumption for a trip input voltage from -0.2 to 0.4 v. The conversion cycle begins at 7 us (subcycle 1 in the first row of the figure) and lasts 4 subcycles. The number of the subcycles is the same as that depicted in Fig. 2. I_{OTA1}, and I_{OTA2} are, respectively, the sum of the two mirror branches bias current and the differential pair bias current for OTA 1 and OTA 2. Table 3 details the values of the bias currents for each OTA and for the ADC in each operation subcycle. The values achieved show the adaptation of the current to the different operating subcycles of the ADC. The fifth column shows the mean value current for the four cycles. The current consumption of the ADC is minimum in the first subcycle, when the input voltage is sampled. Then, as expected, it reaches its peak in the second subcycle, when the OTA 1 is amplifying the residue voltage, to decay again in subcycles 3 and 4. If the bias current adaptation is not implemented, then the ADC would require an average current of 35.24 µA. Thus, this technique means a 34.4 % reduction in the average current.

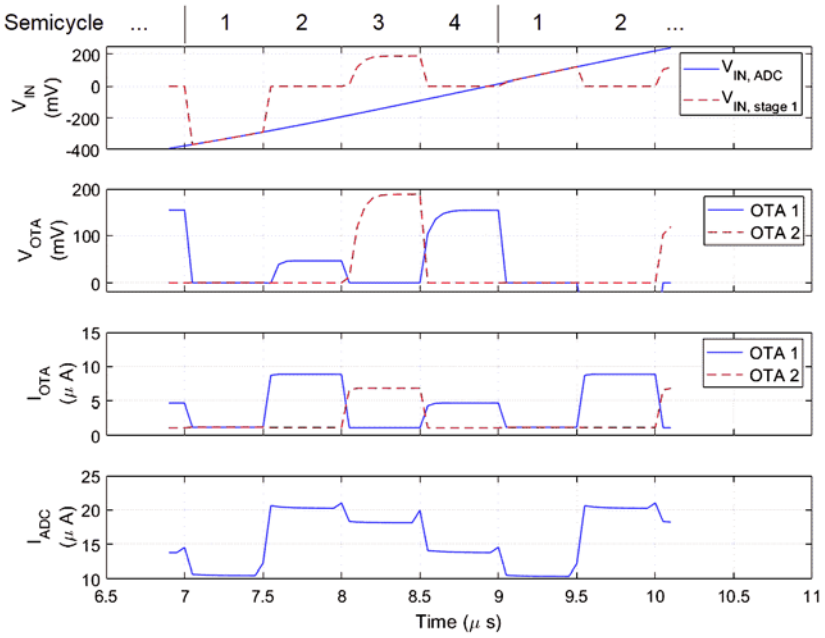

Fig. 6 Evolution of currents and voltages in the OTAs of both stages for 500 kS/s.

Table 3. Total bias current in each subcycle of operation.

	Subcycle				
	1	2	3	4	Mean 1-4
I_{OTA1} (µA)	1.21	8.86	1.14	4.67	3.85
I_{OTA2} (µA)	1.23	1.17	6.82	1.12	2.39
I_{ADC} (µA)	10.52	20.30	18.15	13.82	23.11

Figs. 7 and 8 show the SNDR achieved at schematic level simulations versus input and sampling frequencies. The SNDR was obtained using the IEEE-STD-1241 4-parameters sine wave test. For a sampling frequency of 500 kS/s, the SNDR remains above 55 dB for an input frequency up to 250 kHz. For an input frequency of 56 kHz, the SNDR is above 55 dB, while showing a continuous decrease above 1.2 MS/s.

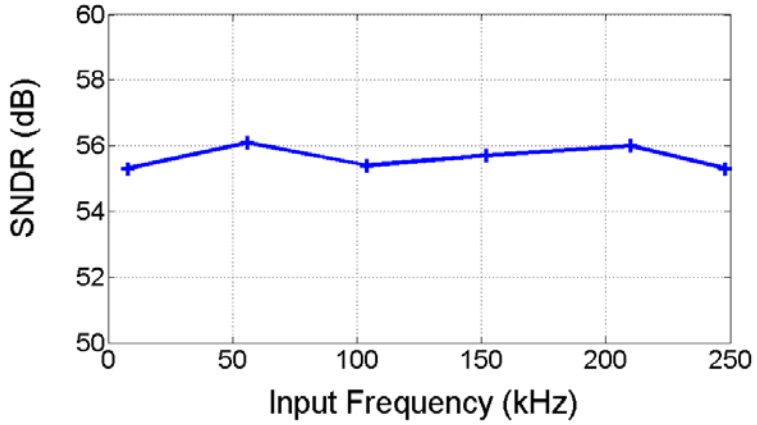

Fig. 7 Dynamic performance of the ADC versus input frequency at fS of 500 kS/s.

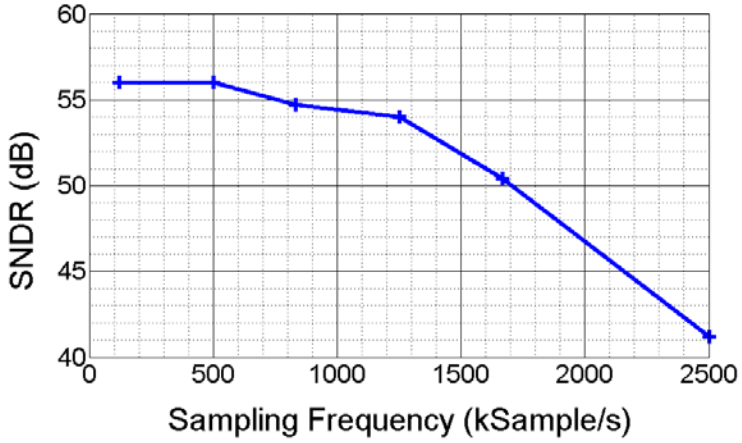

Fig. 8 Dynamic performance of the ADC versus sampling frequency at fIN of 56Hz.

The following Figure of Merit (FoM) has been used to evaluate the performance of the ADC:

$$FOM = \frac{Power}{F_s \cdot 2^{ENOB}} \qquad (7)$$

For a sampling frequency of 500 kS/s, the FoM has been 109 fJ/step. Overall ADC performance is summarized in Table 4, where it is compared with that of other 9-bit cyclic converters. The circuit described in [7] achieves lower power dissipation, but its sampling frequency of 10 kS/s is clearly below the one obtained in this work. On the other hand, the converters described in [2-4] exhibit higher sampling frequencies, but their power dissipation is in the order of magnitude of miliwatts. The combination of the power dissipation, the sampling frequency and the effective number of bits yields a FoM whose smallest value corresponds to the circuit presented in this work.

Table 4. Summarized performance of the cyclic ADC.

Parameter	[3]	[4]	[5]	[6]	[7]	This work
Technology (nm)	90	350	180	350	130	110
Supply Voltage (V)	1	3.3	1.8	3.3	1.4	1.2
Sampling Rate (MS/s)	50	2	16.7	0.01	0.01	0.5
Power (mW)	6.9	1	4.7	0.033	0.011	0.0279
SNDR@(Fs) (dB)	50.5	48	52.5	54.2	52.6	56
ENOB@(Fs) (Bits)	NA	8.2	NA	8.7	8.4	9
FoM (pJ/Step)	$504 \cdot 10^{-3}$	$977 \cdot 10^{-3}$ (1)	$818 \cdot 10^{-3}$	7.94	3.25	$109 \cdot 10^{-3}$
Input Voltage Dynamic Range (Vpp)	NA	1	NA	2	1.4	1.2

(1) Estimated FoM considering ENOB = 9

An alternative comparative of the performance of the ADC described in this paper with the state of art of other ADCs is shown in Fig. 9. The figure plots the FoM versus the sampling frequency of ADCs having different topologies and CMOS technologies. The works have been mainly extracted from the ADC Performance Survey 1997-2017 (ISSCC & VLSI Symposium) [19], for the period 2009-2017, and also include pipeline circuits implementing power scaling methods. The selected ADCs [20-36] have sampling frequencies from 20 kSamples/s to 8 MSamples/s. The result proves that the technique of using a variable bias current based on the specifications of each subcycle and stage can significantly reduce the total power consumption of a cyclic pipeline ADC. The FoM obtained in this work places this ADC very close to the best works included in this survey, even though the figure includes circuits of different topologies and CMOS technological nodes.

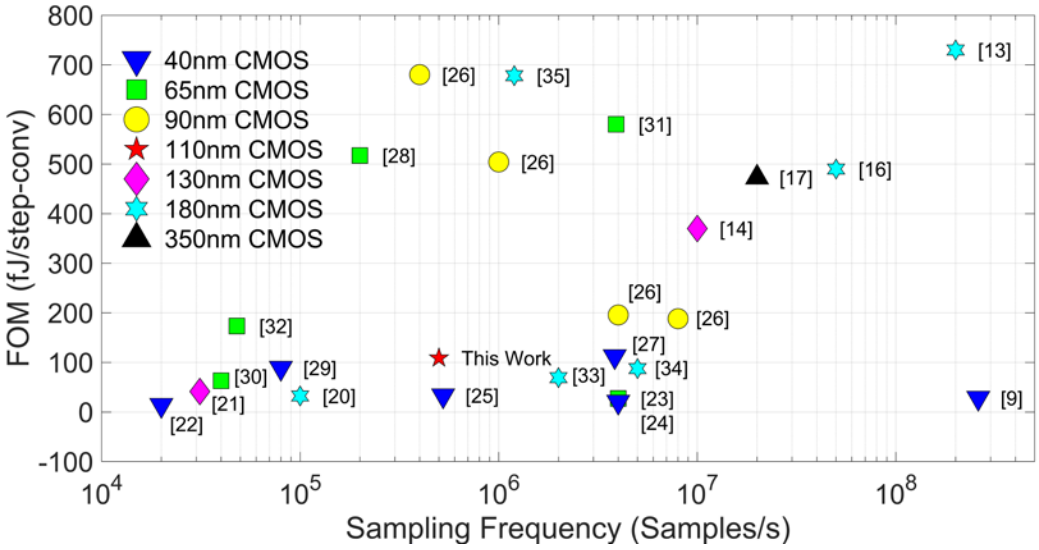

Fig. 9 FoM vs Sampling frequency for ADCs of different topologies and technologies.

4. Conclusion

In this paper, a technique to reduce the power dissipation of a 2-stage cyclic ADC has been described. The proposed architecture regulates the bias current according to the subcycle in which the ADC is operating and the stage which is amplifying. The circuit has been designed in a 110 nm CMOS technology and the simulation results show reduction in the average current of the ADC above 34% compared to a classical design where no regulation is done over the bias current. This technique can be further optimized by exploiting OTA sharing techniques between adjacent stages of the converter. This offers the possibility of improving the FoM in future designs.

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