Influence of the amplifier sharing tecnique in pipeline analog-to digital converters (ADCs)

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Abstract. *Three 12 bit, 40 MS/s pipelined analog-to-digital-converters (ADCs) are developed in 0.35μm CMOS process with 3.3V single power supply. The proposed ADCs architectures study the influence of the amplifier sharing technique in the power consumption and the main performances in the pipeline ADCs. Simulations results with extracted netlists are provided and show that the amplifier sharing technique has potential to be used in the reduction of the power consumption.*

1. Introduction

Power dissipation is a key performance to be considered in all type of portable electronic devices. Most of them (photo and video cameras, mobile phones, etc) contain ADC circuits inside them. Thus, power reduction becomes an essential specification in these circuits. In the case of pipelined ADCs, several techniques have been developed to reduce the power dissipation, although they are basically classified in two main types. One consists in reducing the power dissipation of the operational amplifiers. This can be achieved exploiting stage scaling techniques [1], where switched capacitor (SC) circuits in each stage are determined by noise requirements [2]. It has been proved that thermal noise contribution of a given stage is reduced by the previous stages gain. This allows the reduction of the capacitors size of that stage. The other technique is based on amplifiers sharing [3-5] between adjacent ADC stages working in opposite clock phases. This allows a theoretical reduction of one half in the number of amplifiers. On the other hand, the complexity of the pipeline stage is increased and more clock signals with different phases are needed for the switches of ADC. The effect of the increased complexity on the power consumption is minimal compared to the benefit gained from the amplifier sharing.

In this paper a hybrid amplifier sharing topology is proposed. The two first stages are designed as a conventional pipeline ADC, each one with its own amplifier, while the rest of stages take advantage of amplifier sharing technique. In this way we minimize some of the aforementioned drawbacks, specially the settling time for first stages. In order to evaluate performance of this topology, we have made a comparison with two equivalent converters: one built using fully amplifier sharing and another with a single amplifier for each stage. The structure of this paper is then the following. Section II describes the topologies of the three different pipeline ADCs which are under study. The results obtained for the three topologies are described in section III. Finally we conclude in section IV.

2. Structures under study

In order to test the partial sharing technique, we have selected a 40-MS/s 12-bit pipeline ADC. It is composed by eleven stages working interleaved. They have a conversion schema of 1.5 bit per stage [6], and a Redundant-Signed-Digit architecture (RSD) to obtain the 12 bit output (Figs. 1, 3, 4). To obtain comparable results, we have analyzed three different topologies capable to achieve these specifications. The first one is a common topology without amplifier sharing. In the second topology all stages work with amplifier sharing technique. Finally the third topology is the one we propose, in which amplifier sharing is not used in the two first stages, while it is exploited in the rest of them.

2.1 Pipeline ADC without opamp sharing

In this configuration (Fig. 1) each stage has a Sample & Hold Amplifier (SHA) [7], which is composed of a switch capacitor circuit and operational transconductance amplifier (OTA).

Fig. 1:ADC with conventional scaling.

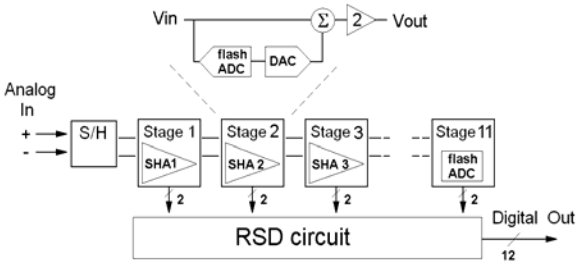
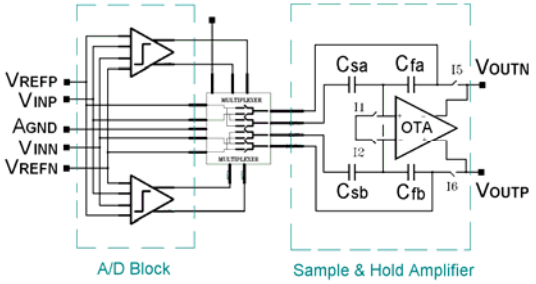


Fig. 2:Single stage topology.



In this ADC both the OTA and the SC capacitors have been scaled depending on their position in the pipeline. The last stage does not require amplification, and it consists only in the pair of comparators, working as a 2 bit flash ADC. Fig. 2 shows the structure of a single stage.

2.2 Pipeline ADC with opamp sharing

Fig. 3 shows the general topology of this ADC, whose stages have been designed using the amplifier sharing technique. With this topology, the number of OTAs is divided by two obtaining a reduction of the power dissipation but adding a complex circuitry in the critical stages. The main difference regarding to a common stage is found in the SHA circuit. This circuit has been simplified and the OTA in Fig 2. has been removed, being now shared between adjacent stages. Thus, every stage contains now the comparators and the SC circuit. The size of the switches I1 and I2 (Fig. 2), the switches to drive signal to the i_{th} amplifier (Fig. 3) and the pair differential of the shared OTA are critical to get the required SNR.

An ADC with resolution higher than 10 bit and a big dynamic range could reduce its SNR or bandwidth if double sampling is used in the first stages.

2.3 Pipeline ADC with partial opamp sharing

In order to minimize the mentioned drawbacks, a mixed topology has been proposed, where amplifier sharing is applied to the stages 3 to 10, while the two first and more critical stages work with their own SHA circuits (Fig. 4). So, the number of OTAs is reduced keeping a robust design according to parameter as SNR and bandwidth.

Fig. 3:ADC with amplifier sharing.

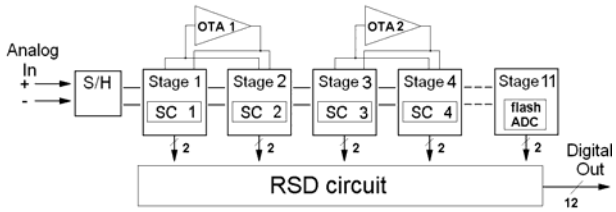
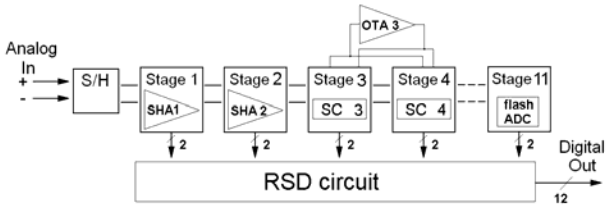


Fig. 4:ADC with partial amplifier sharing.



This topology is focused to minimize effects of additional circuitry in the two first stages, which are the most critical ones. These two stages have also a SHA scaled circuitry and their structure is similar to that show in Fig. 2. Topologies and connections of rest of the stages are the same than those used for the previous circuit.

3. Results

A prototype of the ADC based on the first architecture without amplifier sharing was fabricated in a 0.35 µm CMOS technology (Fig. 5) [8]. The topology with full amplifier sharing has been designed just to obtain comparative results (Fig 6), and at the moment of writing this paper this amplifier was not prototyped. Finally, a prototype of the mixed topology has been recently manufactured, and the measurements in laboratory have not yet been performed. Thus, in this paper, in order to offer comparable measurements, we show the results of the simulations with the parasitic resistors and capacitor (PRC) extractions from the three topologies.

In the three topologies, the technology employed has been AMS CMOS-C35B4. All the input and feedback capacitors have been scaled according to thermal noise, number of bits and dynamic range. For every circuit, there is a generator of clock signals. The bias circuit generator controls and provides all bias currents of the ADC which can be generated from an internal or external master bias current. The RSD algorithm was implemented inside the three ADCs. Besides, the stability of the OTAs, bandwidth and DC-Gain were evaluated through extracted PRC simulations.

Fig. 5:Chip microphotograph of the ADC without amplifier sharing.

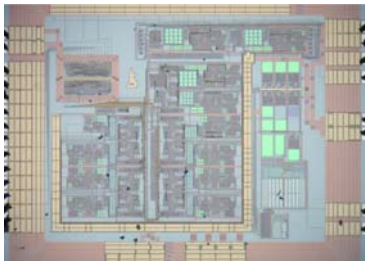
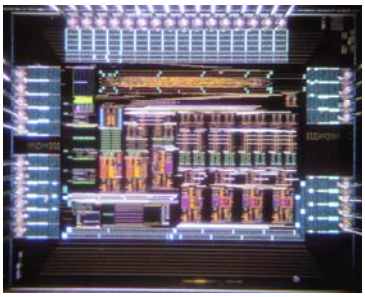


Fig. 6:Chip microphotograph of the ADC with partial OTA sharing.



For the OTA, the telescopic topology was used because it reached better results in phase margin and bandwidth than other topologies as folded cascode when an identical power and capacitance load were required.

Results obtained from PRC extracted simulations of the three ADCs are shown in Tab I. They were obtained using IEEE Std 1241-2000. All three circuits require the same power supply (3.3V) and have been designed for input and output common mode voltages of 1.8V. The input frequency has been 7 MHz and the sampling frequency has been 40 MS/s for the three circuits. As we can see, although the three ADCs offer a similar Signal plus Noise Distortion Ratio (SNDR), ADC3 presents the best relation between SNDR and power consumption. ADC3 presents also a higher robustness because it uses a simplified circuitry in the first stages.

4. Conclusions

We have presented a comparison of three topologies of pipeline ADCs. The first one is a common topology without amplifier sharing but with scaled operational amplifiers and capacitors. In the second topology all stages work with amplifier sharing technique and finally the third one, amplifier sharing is not used in the two first stages. All the OTAs used in the three ADCs are fully differential telescopic circuits with gain boosting and common-mode feedback switched capacitor circuits inside (CMFB). This topology shows a high DC-Gain, a high united gain bandwidth and a fast settling.

Tab. 1:Extracted PRC simulation Results.

	ADC1 No sharing	**ADC2 Full sharing**	**ADC3 Partial sharing**
SNDR (dB)	68.1	66.6	68.7
ENOB	11.06	10.81	11.16
Dynamic Range(Vpp)	3	3	3
Power (mW)	160.9	92.4	107
Linearity error (LSB)	+0.92 / -1.04	+1.77 / -1.2	+1.26 / -0.92
Size (mm^2)	2.26 x 2.54	1.87 x 2.46	1.87x 2.46

The main drawback of amplifier sharing technique comes for the complex circuitry introduced in the design. The switches employed increase series resistance, which yield a higher settling time for each stage. This effect is specially important for the first stages, which are the more critical one in order to achieve required SNR or bandwidth. For this reason, a mixed topology using stage scaling for the first stages, and classical amplifier sharing for the latter ones has been developed. Although the lower power dissipation is achieved employing the amplifier sharing techniques in all the stages of the circuit, the partial amplifier sharing, applied to the latter stages of the circuit exhibits a good tradeoff between circuit resolution and power dissipation.

Acknowledgments

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References

[1] T. Cho, P. R. Gray, ”A 10 b, 20 MSample/s, 35 mW pipeline A/D converter”, IEEE J. Solid-State Circuits, vol. 30, no. 3, pp. 166-172, Mar. 1995.

[2] D. Cline, P. Gray, “A power optimized 13-b 5-Msamples/s pipelined analog-digital converter in 1.2μ CMOS”, IEEE J of Solid State Circuits, vol. 31, pp-294-303, Mar. 1996.

[3] P. C. Yu, H.-S. Lee, ”A 2.5-V, 12-b, 5-Msample/s pipelined CMOS ADC”,IEEE J. Solid-State Circuits, vol. 31, no. 12, pp. 1854-1861, Dec. 1996.

[4] B. M. Min, P. Kim, F. W. Bowman, D. Boisvert, A. J. Aude, ”A 69- mW 10-bit 80-MSample/s pipelined CMOS ADC”, IEEE J. Solid- State Circuits, vol. 38, no. 12, pp. 2031-2039, Dec. 2003.

[5] D. Kurose, T. Ito, T. Ueno, T. Yamaji, T. Itakura, ”55-mW 200-MSPS 10-bit Pipeline ADCs for Wireless Receiver”, IEEE J. of Solid State Circuits, vol. 41, num. 7, July 2006.

[6] A. M. Abo, P. R. Gray, “A 1.5 V, 10-bit, 14-Msample/s CMOS Pipeline Analog-to Digital Converter”. IEEE Jour.. of Solid State Circuits, Vol. 34, No 5. May 1999.

[7] R. J. Baker, “CMOS mixed-signal circuit design”, Wiley-Interscience, 2002.

[8] J.A. Diaz, H. Neubauer, G. Domenech, R. Ruiz “Comparative analysis of two operational amplifier topologies for a 40MS/s 12-bit pipelined ADC in 0.35μm CMOS”, Intl. Conf. on IC Design and Technology, ICICDT’08, Grenoble, 2-4 jun, 2008.