Designing Single-Stage Power Factor Correctors and LC passive filters to Comply with the New Version of the IEC 1000-3-2 Regulations

W. M. Lin[1], J. A. Villarejo[2], J. Sebastian[3], A. Fernandez[3] and M. M. Hernando[3]

[1] Department of Electrical Engineering, Fuzhou University, Fuzhou, Fujian 350002, CHINA

[2] Universidad Politécnica de Cartagena. Departamento de Tecnología Electrónica.
Campus Muralla del Mar. 30202 Cartagena. SPAIN

[3] Universidad de Oviedo. Departamento de Ingeniería Eléctrica, Electrónica, de Computadores y Sistemas.
Grupo de Electrónica Industrial.
Campus Universitario de Viesques. 33204 Gijón. SPAIN
Phone: +34 985 18 20 85. Fax: +34 985 18 21 38.

***Abstract*- The design of low-cost power supplies is influenced by the regulations on the low-frequency harmonic content in the line. As IEC 1000-3-2 regulations have just been modified, the design procedure of low-cost power supplies should also be modified. According to the new version of the above-mentioned regulations, many power supplies classified as Class D in the past are classified as Class A now. This fact allows a remarkable saving in the size of the reactive elements used to reduce the line harmonics if they have been properly designed. The minimum values of the magnetic elements used in two well-known PFC solutions (one is an S²PFC and the other is a passive filter) have been obtained in this paper for equipment classified in both the new Class A and the new Class D and for any power level between 75W and 600W.**

I. Introduction

In recent years, power factor correction circuits [1] have become more and more common in power electronic equipment. There are two main reasons for this:

- The high power factor of the front-end rectifier improves the maximum available power drawn from the line.
- Some regulations have appeared to limit the harmonic content of the line current of mains-connected equipment.

The earliest harmonic standards came from Europe. Some milestones in the development of these regulations are the EN50006 standard (1975), the IEC555 standard (1982) and the EN 60555-2 standard (1991). In 1995, the IEC1000-3-2 Document [2], first edition, was approved as a European standard. In 2000, the second edition document of "draft of the proposed CLC Common Modification to IEC 61000-3-2 Ed. 2.0:2000" [3] was approved, also as a European standard. Therefore, it should be noted that the regulations have just changed.

The aim of this paper is to give information of how two of the low-cost circuits used to comply with the old version of the IEC1000-3-2 regulations must be designed to comply with the new version of these same regulations. The two low-cost solutions analysed in this paper are the following:

- One of the Single-Stage Power Factor Correctors (S²PFC) recently proposed, in particular the one based on the Active Input Current Shapers (AICS) [4-7].
- One of the classical passive solutions, in particular the basic rectifier with LC filter [8, 9].

II. Differences Between the Two Versions of the IEC-1000-3-2 Regulation

Many PFC circuits have been designed at present according to the first edition version of the IEC 1000-3-2 regulations that was published in 1995. However, this standard has been modified in the new edition of the above-mentioned regulations and, as a consequence, these new changes should be taken into account for new designs.

The new standard defines four different classes for power electronic equipment: A, B, C and D (see Fig.1). These classes establish different current harmonic limits depending on the use of the electronic equipment. The most important change in the new regulations is how to classify the Class D equipment. In the first edition, Class D is applied to equipment with a special current waveform that fits within a template defined by the regulations.

In the new standard, the template of the Class D line current waveform disappears. The Class D harmonic limit

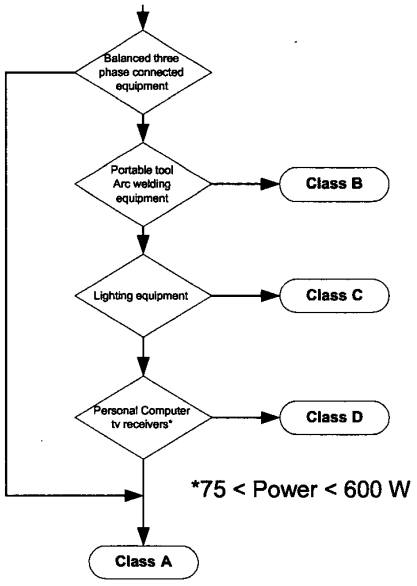

Fig. 1. IEC-1000-3-2 (Ed.2.0:2000) flowchart

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specifications derived from Table I must be applied to equipment with a maximum input power of less than or equal to 600W, of the following types:

1) Personal computers and personal computer monitors.
2) Television receivers.

Therefore, it should be noted that much equipment, which were classified as Class D according to the old version of the regulations, wouldbe classified in Class A according to the new version. For this class, the line current harmonics must not exceed the values given in Table II.

As shown in the new regulations, the Class A harmonic limits allow more distortion at low power levels. Due to this, it is easier to achieve compliance in Class A. Figure 2 shows the ratio of the Class A limits and Class D limits against the input power, over the range of 75W to 600W. It should be noted that only odd harmonics from the 3rd to 15th have been shown in Fig. 2 because the ratios above the 15th are equal to those of the 15th harmonic.

As can be deduced from Fig. 2, the condition to comply with the regulation is quite different according to the new edition of the IEC 1000-3-2 regulations. This is because a piece of equipment classified as Class D in the past can be classified as Class A according to the new version of the regulations. For example, a 200W battery charger is classified now as Class A (whatever the line current waveform is) and, therefore, its maximum allowed level of line harmonic is the same as the one for a 600W battery charger. This means that a simpler (and, therefore, cheaper) harmonic reduction system can be used in the first case. In summary, the harmonic reduction system (passive filter, S²PFC, line-frequency switching active solutions, etc) for pieces of equipment classified now as Class A could be designed at lower cost than in the past, according to the new version of the regulations.

TABLE I. CLASS D HARMONIC LIMITS

Harmonic Order n	Relative Harmonic Limits (mArms/W)	Max. Permissible harmonic current, only for 600W(Arms)
3	3.4	2.30
5	1.9	1.14
7	1.0	0.77
9	0.5	0.40
11	0.35	0.33
13	0.296	0.21
15<n<39	3.85/n	2.25/n

TABLE II. CLASS A HARMONIC LIMITS

Harmonic Order n	Max. Permissible harmonic for any power (Arms)
3	2.3
5	1.14
7	0.77
9	0.40
11	0.33
13	0.21
15	0.15*15/n

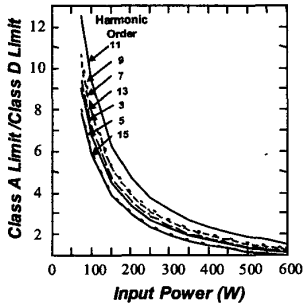

Fig. 2. Ratio of Class A and Class D limits against input power

III. DESIGN OF ACTIVE INPUT CURRENT SHAPERS

In order to comply with the IEC1000-3-2 regulations, many researchers and power supply manufactures have been looking for the most effective and economical solution to mitigate line harmonic due to power supplies. The AICS is the S²PFC proposed in [4-7] (see Fig. 3a) and it is one of the cost-effective active power factor correction solutions. To comply with the standards at the lowest possible cost when the AICS is used to reduce the line-current harmonic content, the size of the delaying inductor L_D and of the filter inductor L_F of the AICS should be minimized. Therefore, it is necessary to obtain the minimum values of L_D and L_F that allows compliance with the regulations as a function of power level.

The design procedure starts by replacing the AICS for the equivalent circuit shown in Fig. 3b, and assuming that the bulk capacitor is so large that its voltage can be considered constant for a line half-cycle and, therefore, the duty-cycle is constant as well. In these conditions, the input current at full load $i_{gPmax}(\omega t)$ (see Fig. 3c) in a line half-cycle can be calculated (by power balance) as follows:

$$i_{gPmax}(\omega_L t) = \frac{2\cdot\pi\cdot P_{max}\cdot\left(\sin(\omega_L t)-\cos(\varphi_c/2)\right)}{\left(\varphi_c-\sin(\varphi_c)\right)\cdot V_g} \quad \text{if} \quad \frac{\pi-\varphi_C}{2} < \omega_L t < \frac{\pi+\varphi_C}{2} \quad \text{1a),}$$

and

$$i_{gPmax}(\omega_L t) = 0 \quad \text{if} \quad \omega_L t < \frac{\pi-\varphi_C}{2} \quad \text{or} \quad \omega_L t > \frac{\pi+\varphi_C}{2} \quad \text{(1b),}$$

where P_{max} is the maximum input power, ϕ_c is the conduction

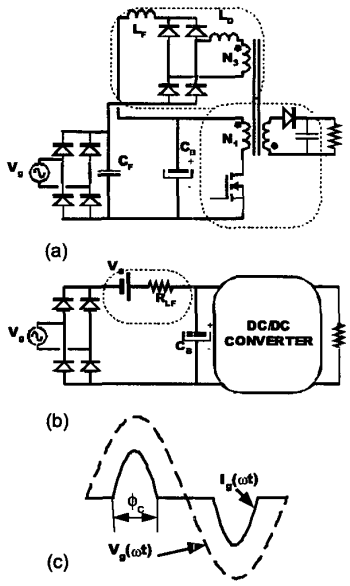

Fig. 3. a) Flyback AC/DC converter with AICS. b) Equivalent circuit. c) Input current waveform

angle, V_g is the peak value of nominal input voltage and ω_L is the angular frequency of the line.

Once the line current waveform has been determined as a function of the conduction angle, its harmonic content for each conduction angle can be easily calculated by using Fourier analysis. Each one of these harmonics must be lower than the limit value specified in the regulations for each one of them. The minimum conduction angle compatible with compliance with the regulations will be obtained by equalling the value of the more restrictive harmonic (which is a function of the conduction angle, as in the case of any harmonic) to the limit value specified in the regulations. Once the minimum value of ϕ_c compatible with compliance with the regulation is known, then the value of L_D can be calculated as follows [4,6]:

$$L_D = \frac{V_g^2 \cdot (\varphi_c - \sin(\varphi_c))}{2 \cdot \pi \cdot P_{max} \cdot f_S \cdot K} \quad (2),$$

where f_s is the switching frequency and K is a coefficient determined by the AICS topology (K=4 for the AICS shown in Fig. 3a).

As far as achieving compliance with the IEC 1000-3-2 when the equipment has been classified in Class D is concerned, the conditions are very simple: the converter must be designed in such a way that the conduction angle at 230 Vac and at full load is wider than 64.47° (see [4]). This value was obtained in [4] by assuming that the value of the bulk capacitor C_B is large enough to allow us to neglect its voltage ripple. The theoretical result obtained is very close to the experimental results measured in several prototypes [4-6] (even with different values of the bulk capacitor) and, therefore this easy method can be used to design AICS complying with the IEC 1000-3-2 in Class D.

Regarding the conditions to achieve compliance with the IEC 1000-3-2 when the equipment has been classified in Class A, a similar procedure can be followed. If a very large value of the bulk capacitor C_B is assumed, then the input current waveform would have been like the one shown in Fig. 4a (solid lines) for the particular case of a 100 W converter. However, if a moderate value of the bulk capacitor C_B had been assumed (47 μF in the case of a 100 W converter), then the input current waveform would have been as the one shown in Fig. 4a in dotted lines. It should be noted that both waveforms are quite different and, therefore, the harmonic content in both cases will be very different, as well. Fig. 4b shows this fact.

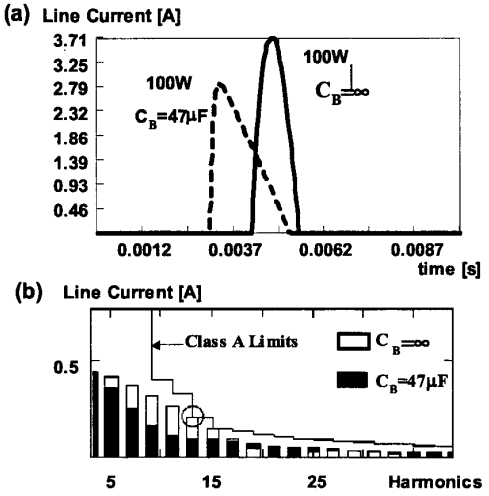

Fig. 4. a) Input current waveform in Class A. b) Harmonic content.

The question at this point is: why is the influence of C_B negligible in Class D and not negligible in Class A? The reason is the following: Due to the fact that the limits in Class A are absolute values (instead of relative values), the conduction angle ϕ_c needed to comply with the regulations for low power converters is very small. This fact allows the optimisation of the AICS because only a very small part of the energy handled by the converter transformer has to be recycled to shape the line current. However, when the converter has been designed to have a very small conduction angle, the value of the bulk capacitor C_B has a strong influence on the actual value of the conduction angle due to the voltage ripple across it. This is the same situation as when a capacitor filter is used: the real conduction angle strongly depends on the filter capacitor value. Fortunately, the line harmonic content with an infinite value of the bulk capacitor is higher than in the case of having a moderate value. Therefore, if we design the converter assuming an infinite value of C_B, then the actual harmonic content with a moderate value of C_B will be lower than in the first case and, therefore, the compliance with the regulations is guaranteed. This means that we can choose C_B according to the desired value of the converter hold-up time, without taking into account the influence of C_B in the harmonic content.

Once we know that we can design the AICS assuming an infinite value of C_B, the design procedure is very similar to the one shown in [4-6] for converters in Class D. The only difference is that the conduction angle needed here is not constant, but it depends on the power instead. The higher the power, the higher the conduction angle should be. Figure 5 shows the relationship between both quantities for different values of C_B. The curves shown in this figure have been obtained maintaining the ratio "capacitance of C_B"/"converter input power" constant. This figure shows that for a given input power, higher values of the conduction angles can be achieved when the value of C_B is decreased. However, as we have explained before, we will assume infinite value of C_B (which is the worst case) in order to continue with the design procedure. In fact, the curves shown in Fig. 6 have been obtained from this assumption. The equivalent elements R_{LF} and V_S can be calculated from these curves. The values of the delaying inductor L_D and of the turns ratio of the additional transformer winding N_1/N_3 can be easily obtained from the following equations [4-6]:

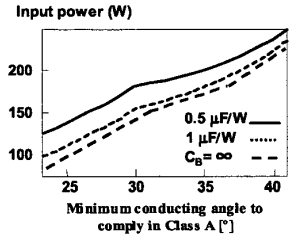

Fig. 5. Minimum conduction angle to comply in Class A against input power.

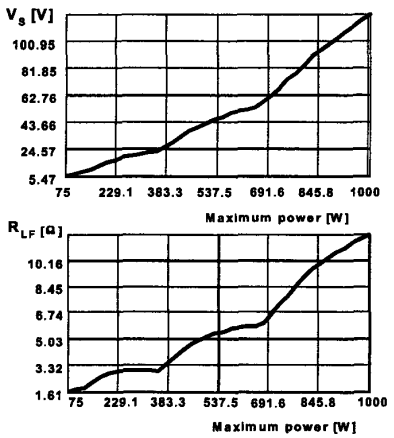

Fig. 6. Values of V_S and R_{LF} against maximum input power

$$L_D = \frac{R_{LF}}{K \cdot f_S} \tag{3}$$

$$\frac{N_1}{N_3} = \frac{\beta \cdot d_{max} \cdot V_{gmin}}{V_S} \tag{4}$$

where K=1 for AICSs based on half-wave rectifiers and K=4 for the AICS shown in Fig. 3a (which is based on a full-wave rectifier), d_{max} is the maximum duty cycle and β=1 for AICSs based on half-wave rectifiers and β=2 for any AICS based on full-wave rectifiers.

Table III shows the inductor values needed to comply with Class A IEC 1000-3-2 for a power range between 100 W and 600 W. The core sizes and the power losses in the inductors are also shown. As can be seen, the core sizes needed are very small, even for 600 W. However, it should also be noted that four additional diodes are needed, as well as an additional winding in the transformer.

Table IV shows the values and the sizes of the inductors but here to comply with the regulations in Class D. As can be seen, the size of the inductors is slightly higher in some cases but in general, the size is the same. However, as the inductance value is higher, the copper losses are also higher.

TABLE III. AICS INDUCTOR VALUES AND CORE SIZES TO COMPLY WITH IEC 1000-3-2, CLASS A

Power (W)	I_{PEAK} (A)	I_{RMS} (A)	L_D=L_F (*) (μH)	Core size	Losses (W)
100	4.079	1.142	4.378	2xE13	2x0.005
200	5.431	1.835	6.967	2xE13	2x0.05
300	6.942	2.538	7.462	2xE13	2x0.177
400	7.651	3.057	9.632	2xE16	2x0.15
500	8.155	3.574	13.02	2xE16	2x0.386
600	8.907	4.095	14.41	2xE20	2x0.33

(*)According to [7], L_D=L_F

TABLE IV. AICS INDUCTOR VALUES AND CORE SIZES TO COMPLY WITH IEC 1000-3-2, CLASS D

Power (W)	I_{PEAK} (A)	I_{RMS} (A)	L_D=L_F (*) (μH)	Core size	Losses (W)
100	1.41	0.66	98	2xE13	2x0.07
200	2.82	1.32	49	2xE13	2x0.35
300	4.23	1.98	33	2xE16	2x0.22
400	5.64	2.64	25	2xE16	2x0.4
500	7.05	3.30	20	2xE20	2x0.2
600	8.47	3.97	16	2xE20	2x0.3

(*)According to [7], L_D=L_F

Finally ,it should be noted that the efficiency penalty that is seen in the converter when the AICS is used is due, not only to power losses in the inductors and the diodes but also to the fact that the energy that is processed by the delayed output will be processed twice. However, as the amount of recycled energy is very small (about 5 % of the input power), the penalty will also be small as will be shown later.

IV. DESIGN OF PASSIVE SOLUTION

In many low and medium power applications, low cost is a primary concern and since IEC 1000-3-2 regulations have been applicable, low cost solutions to reduce the input current harmonic content are one of the hottest topics in power electronics. Single Stage topologies, like the AICS shown before are very popular solutions. Another very interesting option is to use a passive filter to reduce the harmonic content. A simple LC filter can be used to meet IEC 1000-3-2 regulations if the inductance value is properly chosen.

It should be noted that inductor L is the only additional component that should be used. The capacitor can be exactly the same as in a conventional AC/DC converter with just a capacitive filter. It should also be noted that this capacitor is usually designed to meet some hold-up time specifications, typically 10 μs at nominal input voltage or 20 μs at minimum input voltage, which is a more restrictive option.

Thus, the passive solution is very simple, very robust and also very cheap. Moreover, the redesign cost of the power supply is minimum.

Obviously, as there are no new switching components, no EMI is produced by the harmonic reduction system (the LC filter). The inductor operates at the line frequency (50 Hz, or 60 Hz) and hence, it will be built with a silicon steel lamination core. This is probably the key point to use this solution because this type of cores is quite big and their weight is also quite high. Therefore, the minimum inductor needed to comply with the regulations should be calculated and then, the minimum necessary core should be chosen in order to reduce size, weight and cost as much as possible.

Class A and Class D results are quite different because the limits of both classes have different philosophies. As has been already mentioned, Class A limits are absolute and Class D limits are relative.

A. Designing an LC filter to comply with Class A limits.

Fig. 7b shows the typical input current waveform obtained with an LC filter. As Class A limits are not very restrictive for low power levels, the conduction angle ϕ_c needed to comply with IEC 1000-3-2 is quite narrow. As a consequence, the value of the bulk capacitor has a strong influence on the current waveform and hence, on the minimum inductance value needed. Pspice can be used to simulate the circuit shown in Fig. 7a and to calculate the harmonic content of the input current.

In order to obtain practical values, the capacitor was designed to meet the hold-up time specifications. Three values were used to cover a broad range of specifications: 0.5 μF/W, 1 μF/W and 2 μF/W. The results obtained are shown in Fig. 8. As can be seen, the higher the power, the higher the inductance.

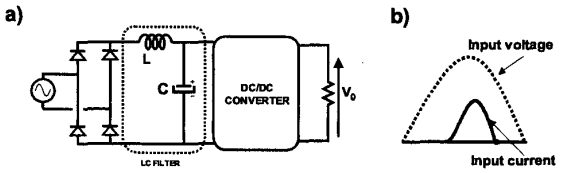

Fig. 7. a) LC filter. b) Input current.

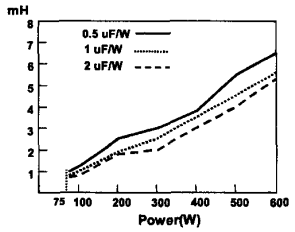

Fig. 8. Minimum value of L against input power (Class A).

The influence of the capacitor can also be seen. The greater the capacitor, the lower the inductance.

To calculate the core needed for each power level, the total losses on the inductor (copper losses + iron losses) were set to be lower than 2% of the total input power. Thus, the efficiency penalty due to the harmonic reduction will be only 2 points.

Table V shows the equivalent standard E core size used (codes for silicon steel lamination cores are different) and the inductor losses (shown as a percentage of the input power). As can be seen, cores smaller than a standard E 34 can be used for up to 300W. This size is really small for these power levels and this makes this solution very attractive. For higher power levels, the core needed is more or less an E 42. This size is not to big but maybe too heavy.

B. Designing an LC filter to comply with Class D limits.

A similar process was followed to obtain the minimum inductance value to comply with the Class D limits. Fig. 9 shows the final results. As can be seen, in this case the higher the power, the smaller the inductance. Moreover, as the conduction angle is wider, the influence of the capacitor is smaller. The average value is shown in Fig. 9.

TABLE V. INDUCTOR VALUE AND CORE SIZE TO COMPLY IEC-1000-3-2, CLASS A WITH AN LC FILTER

Nominal input power (W)	L(mH)	I_{peak}(A)	I_{RMS}(A)	Equivalent ferrite core size	Power losses (%)
100	0.85	3.57	0.94	E20/10/5	0.53
200	1.5	5.28	1.62	E30/15/7	0.8
300	2.4	6.34	2.17	E42/21/15	0.3
400	2.8	7.67	2.78	E42/21/15	0.66
500	4.8	7.41	2.92	E42/21/20	0.57
600	6	8.78	3.7	E42/21/20	1.66

TABLE VI. INDUCTOR VALUE AND CORE SIZE TO COMPLY IEC-1000-3-2, CLASS D WITH AN LC FILTER

Nominal input power (W)	L(mH)	I_{peak}(A)	I_{RMS}(A)	Equivalent ferrite core size	Power losses (%)
100	41	1.5	0.61	E42/21/15	1
200	21	2.9	1.22	E42/21/15	2
300	14	4.35	1.84	E42/21/20	1.1
400	10	5.68	2.46	E42/21/20	1.25
500	8.7	7.28	3.07	E42/21/20	1.8
600	6.9	8.72	3.7	E55	1

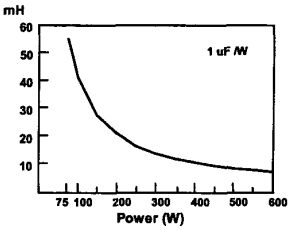

Fig. 9. Minimum value of L against input power (Class D).

Table VI shows the core size used for each power level. It should be noted that the criteria used to calculate these cores is exactly the same as in the previous case, that is, to keep the power losses below 2% of the input power.

As the inductance value needed to comply with the regulations at low power levels (say power < 300 W) is quite high, the core needed is quite big) and hence, this solution is not too attractive for these power levels. For example, a 41 mH inductor is needed for a 100 W application and in this case, a standard E42/15 is used. The power losses are 1%. As can be seen, a silicon steel lamination core of this size is too bulky for such a low power application. However, for higher power levels the size is kept more or less constant and the solution becomes more attractive. An E 55 core can be used for 600 W and the power losses will be only around 1%. It should be noted that these results are a consequence of the geometric characteristics of the E cores used for this comparison.

V. COMPARISON OF THE TWO SOLUTIONS

Two low cost solutions to comply with the new version of IEC 1000-3-2 have been studied: a passive solution and a single stage solution. Both of them are very attractive for low power, low cost applications. However, there are some differences between them.

The passive solution only needs one additional element: a silicon steel laminated core inductor. Then, the extra cost is very small. This solution seems to be very interesting if the piece of equipment is classified into Class A. In this case, the size of the inductors is quite small for the power range between 100 W and 600 W and especially for the power range between 100 W and 300 W.

On the other hand, the LC filter is not so attractive if the application belongs to the Class D and the power is lower than 300 W. In this case, the size of the inductors is quite big for this power level. It should be noted that E42 silicon steel lamination core is needed to comply with the regulations in a 100 W application. For a higher power level (300 W < P < 600 W), the solution becomes more interesting because the size of the inductor is more similar to the one needed to comply in Class A and is more reasonable for that power level.

The efficiency penalty of this solution is only due to the inductor losses. In our case, the inductors have been designed in order to have a power loss lower than 2 % of the input power.

The single stage solution is also very attractive for this type of applications. The topology is slightly more complex (two inductors, four diodes and an additional winding). However, the inductors are designed for high frequency operation and

hence, they are very small as shown in Table III and Table IV. The efficiency penalty of this solution is not only due to the losses in the additional components but also to the fact that about 5 % of the total energy is processed twice. However, this penalty is in general around 2 % - 3 %.

For Class A and a power level of less than 300 W, this solution has a very similar performance to the LC filter. In both cases the efficiency penalty is very small (less than 1%) and the size is also very small. For a higher power level, the size and specially the weight of the single stage solution is smaller.

For Class D, the AICS has in general a better performance, especially at low power because the size of the active solution is much lower than the passive one and the efficiency penalty is more or less the same. However, it should also be noted that in this case, the voltage across the bulk capacitor increases well above the peak input voltage and hence, the capacitor needs a higher voltage rating. This is due to the fact that the amount of recycled energy is higher to comply in Class D than in Class A.

VI. Experimental Results

Two prototypes of the same Flyback ac-to-dc converter have been designed, built and tested. One of them is based on an AICS and the other is based on an LC filter. The main converter characteristics are the following: line voltage = 230 V, 50 Hz; input power 100 W; output voltage = 48 V, switching frequency = 100 kHz. The prototypes were designed to comply with the regulations in both Class A and Class D. The inductor values needed for each case are shown in Table VII.

Table VII: Comparison of experimental results of both solutions

		Inductance	Core Size	Losses (W)	Efficiency penalty
Passive Class A	L_{50Hz}	1.7 mH	E20/10/5	0.5	0.5 %
AICS Class A	L_D=L_F	4.7 μH	2xE13	2x0.005	0.1 %
Passive Class D	L_{50Hz}	41 mH	E42/21/15	1	1 %
AICS Class D	L_D=L_F	98 μH	2xE13	2x0.07	2 %

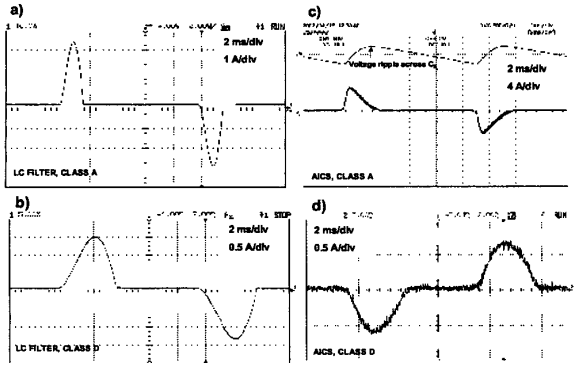

Fig. 10. Iput current waveforms obtained in the four prototypes. a) LC filter and Class A. b) LC filter and Class D. c) AICS and Class A (C_B=47μF). d) AICS and Class D (C_B=47μF)

Figure 10 shows the experimental input current waveforms for the four cases shown in Table VII. The harmonic content obtained in all cases is below the limits specified by the standards. Regarding the case of an AICS designed to operate in Class A (Fig. 10.c), the experimental results fit very well with the predicted ones (see Fig. 4.a). The rest of the waveforms also fit with the theoretically predicted ones in [4-6, 8].

VII. Conclusions

The design of low-cost power supplies is influenced by the regulations about the low-frequency harmonic content in the line. Due to the fact that the IEC 1000-3-2 regulations have just been modified, the design procedure for low-cost power supplies should also be modified. According to the new version of the above-mentioned regulations, many power supplies classified as Class D in the past are classified as Class A now. This fact allows a remarkable saving in reactive elements in proper new designs for low-power equipment, because Class A is less restrictive than Class D for power levels lower than 600W. The minimum values of the magnetic elements used in two well-known PFC solutions (one is an S^2PFC and the other is a passive filter) have been obtained in this paper for equipment classified in both the new Class A and the new Class D and for any power level between 75W and 600W.

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